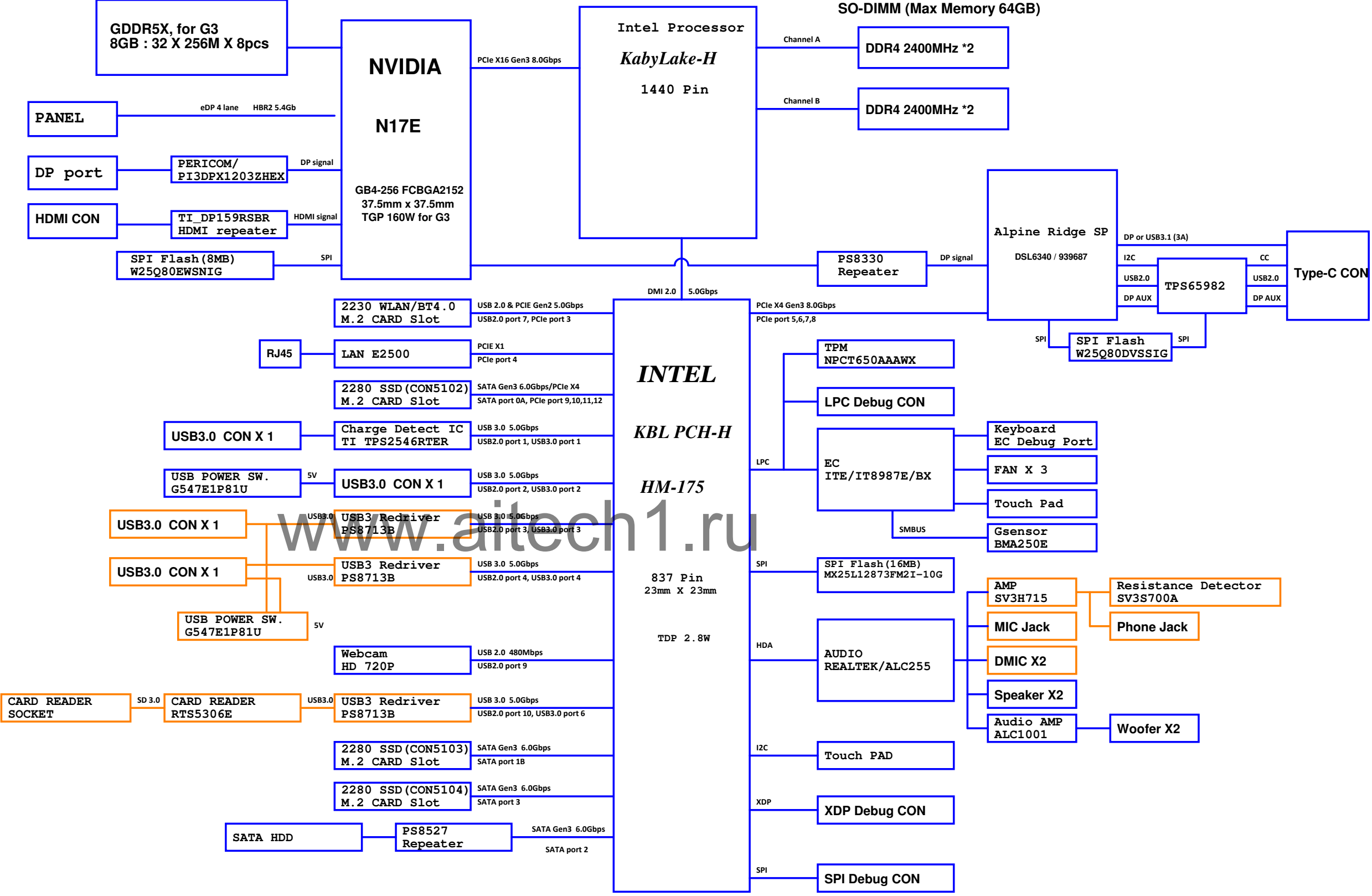


Viper2

PAGE	TITLE
01	BLOCK DIAGRAM
02	CLOCK DISTRIBUTION
03	CPU DDI/EDP
04	CPU DDR4 A
05	CPU DDR4 B
06	CPU DMI/PEG
07	CPU MISC
08	CPU VSS
09	CPU POWER1
10	CPU POWER2
11	Thunderbolt
12	TPS65982/TYPE-C
13	Thunderbolt HDMI redriver
14	Thunderbolt DP redriver
15	xxxThunderbolt
16	DDR4 SO-DIMM0
17.	DDR4 SO-DIMM1
18	DDR4 TERMINATION A&B
19	xxxxxxxxxxxxxxxxxxxxxxxxxxxx
20	PCH DMI PCIE USB SATA 1-8
21	PCH SATA/PCIE 2-8
22	PCH ESPI/SPI/FAN/HOST 3-8
23	PCH AUDIO/CL/I2C/UART 4-8
24	PCH SML/I2C/MISC 5-8
25	PCH CLOCK 6-8
26	PCH VCC/PLL 7-8/RTC
27-28	PCH VSS 8-8
29	xxxCLK
30	EC ITE8987
31	KB/TP/SPI ROM
32	xxxREST IC
33	LAN E2400
34	RJ45 CONNECTOR
35	xxxLAN
36	AUDIO CODEC ALC255
37	AUDIO AMP ALC1001
38	xxxAUDIO
39	xxxAUDIO
40	xxxCB /EXC
41	xxxCB /EXC
42	xxxCB /EXC
43	WEB CAM/3D CAM
44	DEBUG CON
45	EDP/DMIC/TS/LGF
46	DP Multiplexer
47	xxxDVI/DP
48	HDMI OUT
49	xxxHDMI
50	FAN/THERMAL
51	SATA/ODD/SSD CONNECTOR
52	USB CHARGE IC
53	NGFF WLAN
54	xxxBAR
55	USB 3.0 CONNECTOR
56	PWR BOARD CON
57	GPU POWER Discharge
58	G-SENSOR
59	xxxGPS
60-63	BAT CON AC CON/ BOARD ID/ TMP
64	xxxxxxxxxxxxxxxxxxxxxxxxxxxx
65	xxxME
66	xxxESA
67	IO Board/USB SD AUDIO
68	xxxGHS
69	Screw hole
70	N17E-G3_PCIE
71	N17E-G3 Buffer A
72	N17E-G3_DACAand XTAL
73	N17E-G3_Multi-use IO(MIO)
74	N17E-G3_Misc-GPIO_I2C_ROM
75	GPU NVVDD, FBVDDQ, and GND
76	GDDR5/5X 256M x 16bit x 2pcs_TOP1
77	GDDR5/5X 256M x 16bit x 2pcs_TOP2
78	GDDR5/5X 256M x 16bit x 2pcs_BOT1
79	GDDR5/5X 256M x 16bit x 2pcs_BOT2
80	POWER_44e_45W_CORE_GT_SA
81	POWER_SYSTEM
82	POWER_+1.0VSUS
83	POWER_DDR & VTT
84	POWER_+1.5VS
85	POWER_XXX
86	POWER_+1V8_AON
87	POWER_+NVDD (VGA_VCORE)
88	POWER_CHARGER
89	POWER_+FBVDDQ
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_VCCIO
95	POWER_+2.5V
96	POWER_PEX_VDD
97	POWER_+NVDDS
A01	DB_LED

Viper2 (KabyLake-H)

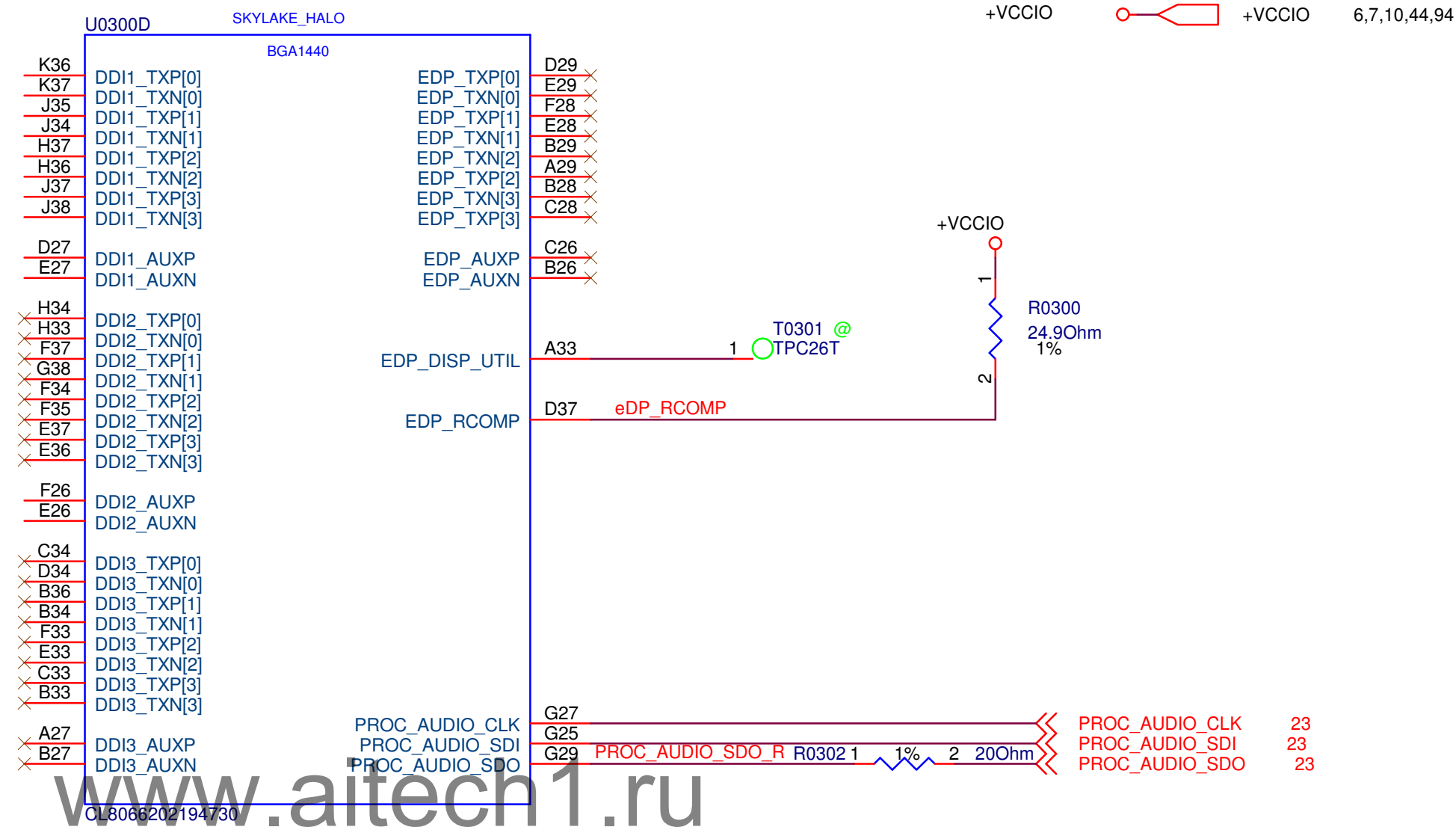
Revision_1.00_2016/05/23

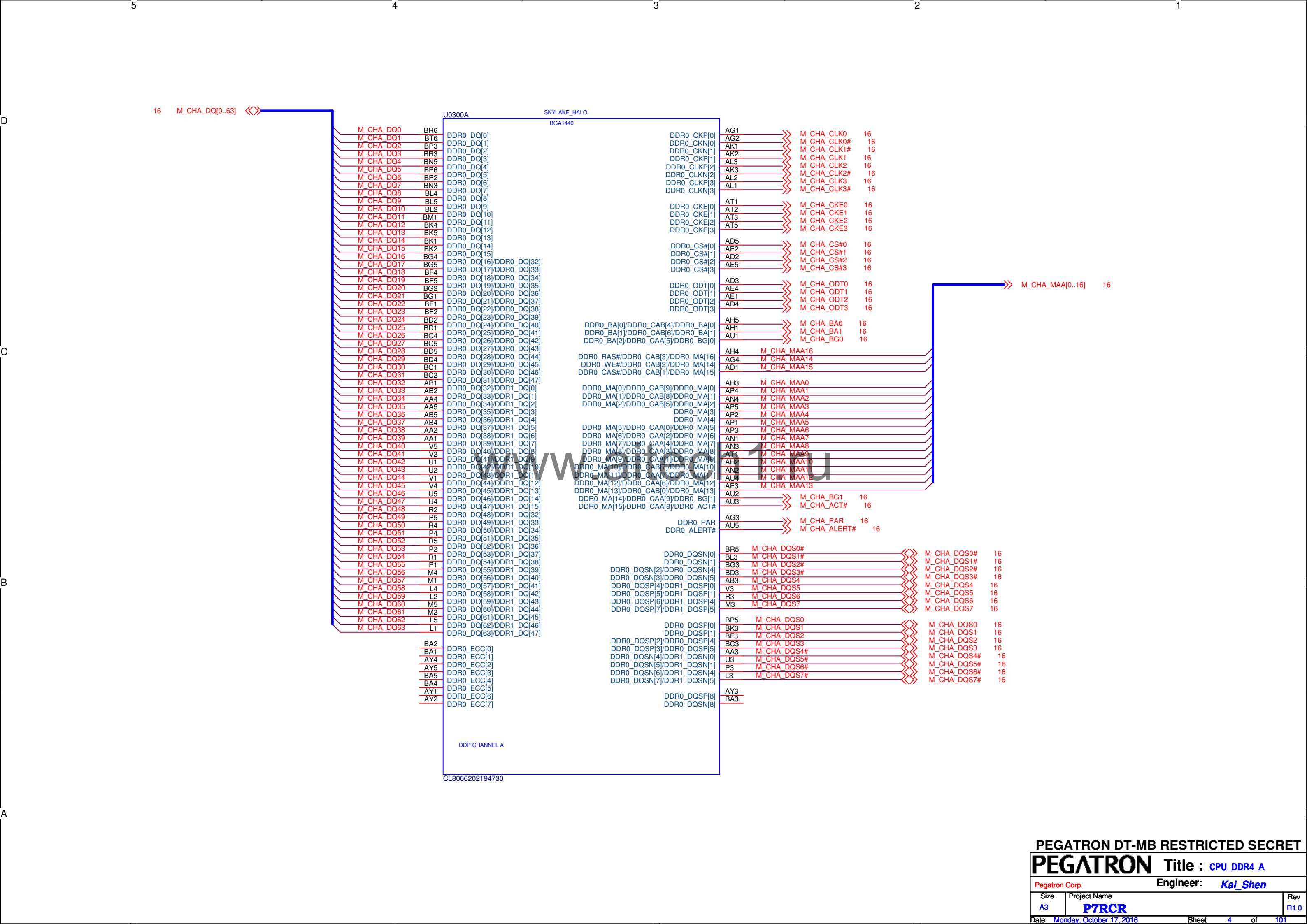


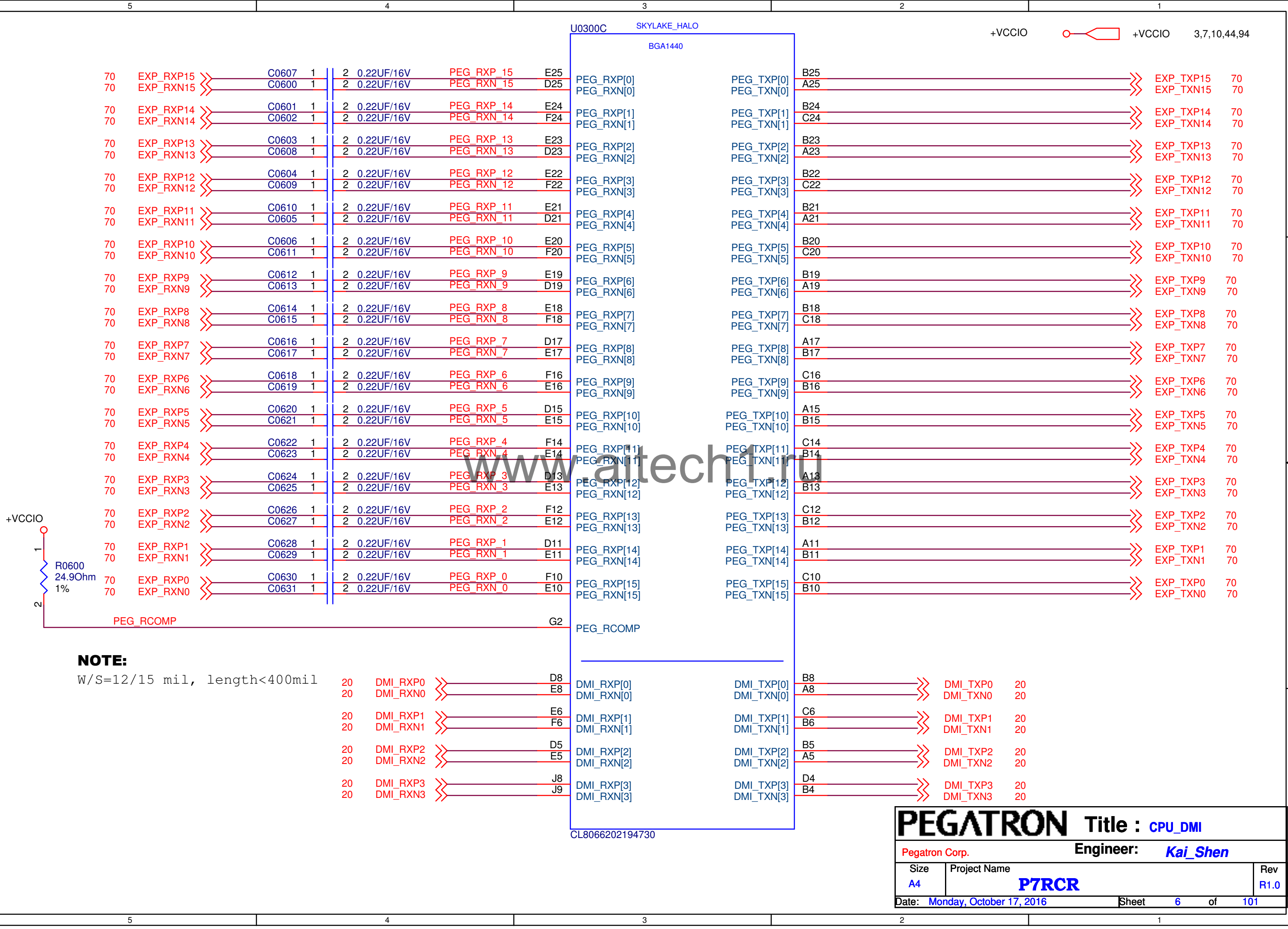
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : BLOCK DIAGRAM	
Pegatron Corp.		Engineer: Kal_Shen	
Size	Project Name	Rev	
Custom	P7RCR	R1.0	
Date: Monday, October 17, 2016		Sheet 1 of 101	

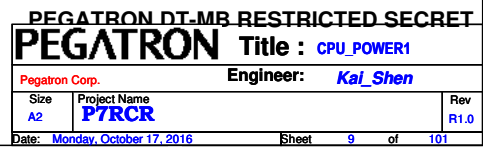
I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		0X2C
I2C_1	TOUCH PANEL		
SMBUS	DDR Channel A(CON1600)		
	DDR Channel A(CON1601)		
	DDR Channel B(CON1700)		
	DDR Channel B(CON1701)		
	Resistance Detector	SV3S700A	0X73
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24735RGRR	0X09
SMBUS1 (EC)	G-SENSOR	BMA250E	0X18
	THERMAL-SENSOR	G781P8F	0X4C
	LED DRIVER	TLC59116IPWR	0X68
	GPU	N17E-G3	0X4F

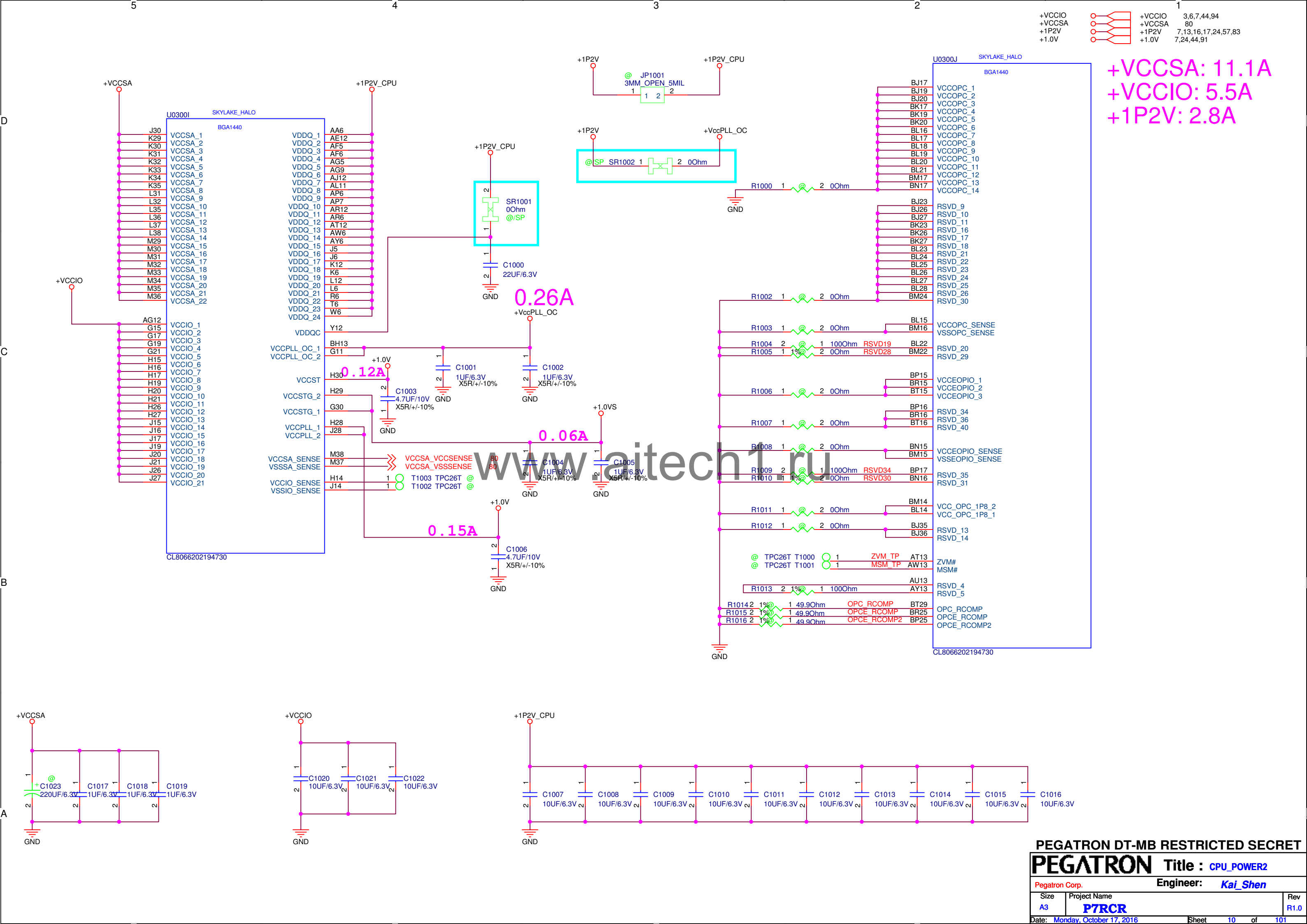








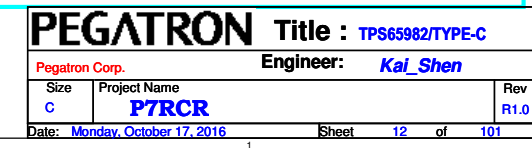








+3VS			+3VS	7,11,13,14,15,16,21,22,23,24,26,30,31,36,45,46,50,51,53,56,58,61,62,67,70,91,92
+3VSUS			+3VSUS	7,11,21,22,23,24,26,28,31,33,36,44,52,53,57,62,67,81,88,92
+3V3_FLASH			+3V3_FLASH	11
+5VSUS			+5VSUS	36,37,45,52,55,56,57,67,81



[I2C_EN_PIN = 0] pin strap mode			
Net / Level	H	L	NC
PRE_SEL	Reserved	-2 dB	0 dB
EQ_SEL_A0	Fixed at 14 dB	Fixed at 7.5 dB	Adaptive EQ
SLEW_CTL	fastest data rate	5 ps slow	10 ps slow
HDMI_SEL#_TEST_A1	DVI	HDMI	N/A

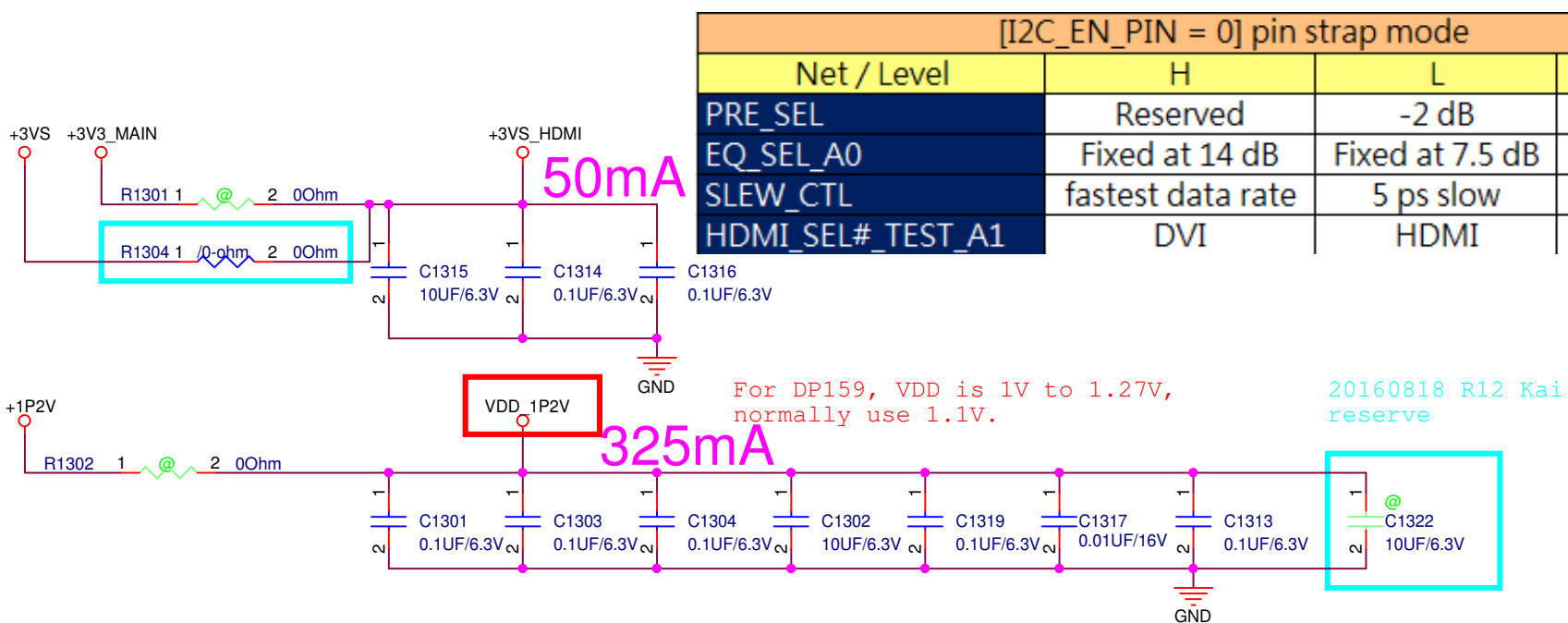
+1P2V 7,10,16,17,24,57,83
+3V3_MAIN 14,57,72,74,87,91,97
+3VS 7,11,12,14,15,16,21,22,23,24,26,30,31,36,45,46,50,51,53,56,58,61,62,67,70,91,92
+5VS_HDMI 48

[DP159 DDC on]
mount R1306 / R1307 / R1312 / R1313 / R7227 / R7228,
unmount R1308 / R1309 / R1310 / R1311 / R7225 / R7226 / Q7205 / Q7206.

[DP159 DDC snoop only] bypass I2C clock strength
unmount R1306 / R1307 / R1312 / R1313 / R7227 / R7228,
mount R1308 / R1309 / R1310 / R1311 / R7225 / R7226 / Q7205 / Q7206.

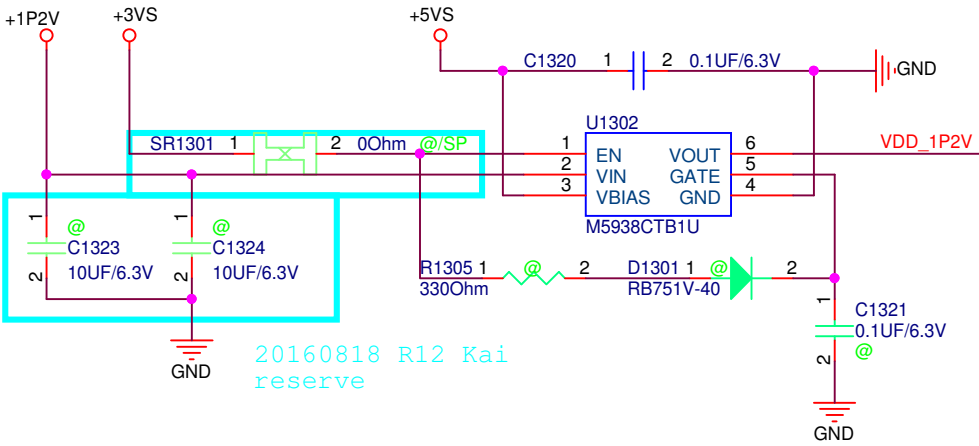
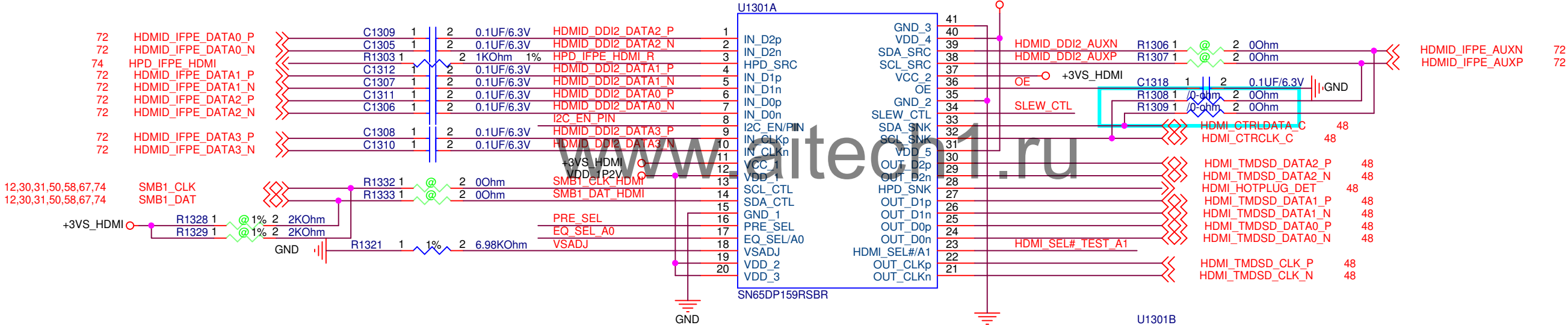
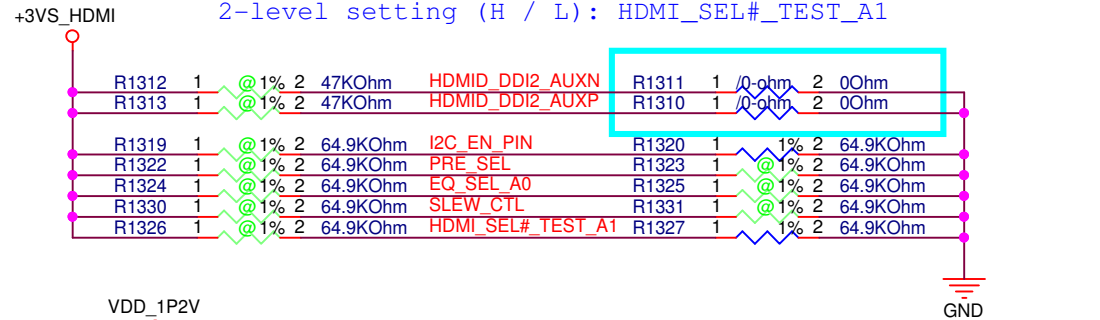
[I2C_EN_PIN = 1] I2C control mode
unmount R1320, mount R1319 / R1328 / R1329 / R1332 / R1333,


[I2C_EN_PIN = 0] pin strap mode
mount R1320, unmount R1319 / R1328 / R1329 / R1332 / R1333,
3-level setting (H / L / NC): PRE_SEL / EQ_SEL_A0 / SLEW_CTL
2-level setting (H / L): HDMI_SEL#_TEST_A1

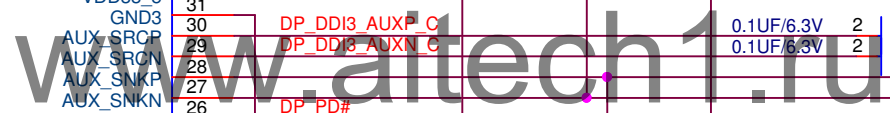
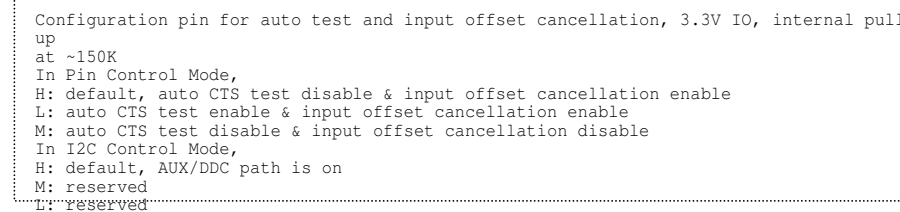
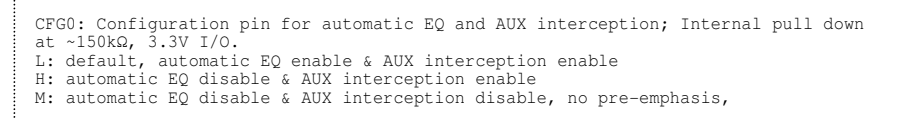
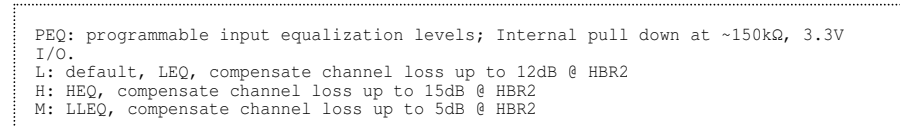


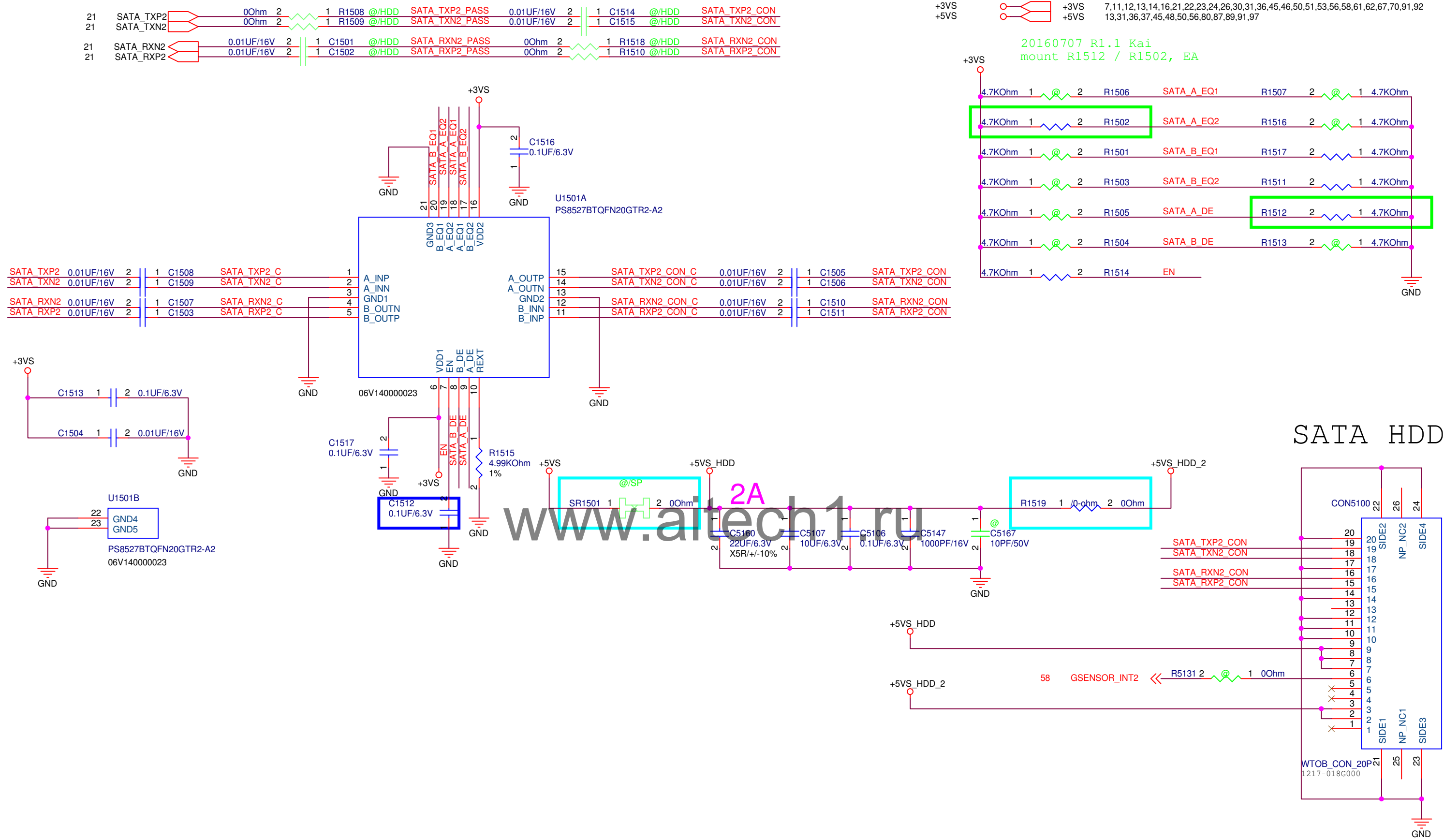
20160512 WS Kai
SWAP Port 0 / 2, follow NV HDMI output port

20160523 WS Kai
Recover R1303 to 1k-ohm

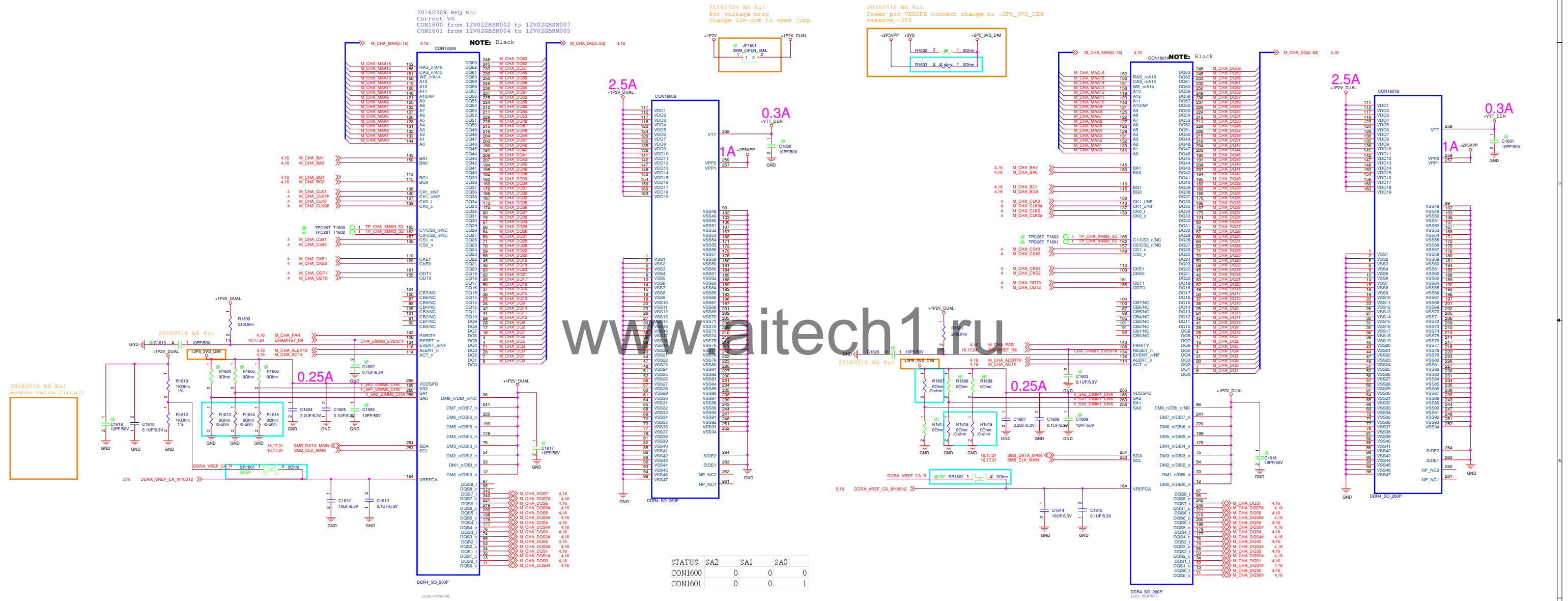


+3V3_MAIN		+3V3_MAIN	13,57,72,74,87,91,97
+3VS		+3VS	7,11,12,13,15,16,21,22,23,24,26,30,31,36,45,46,50,51,53,56,58,61,62,67,70,91,92

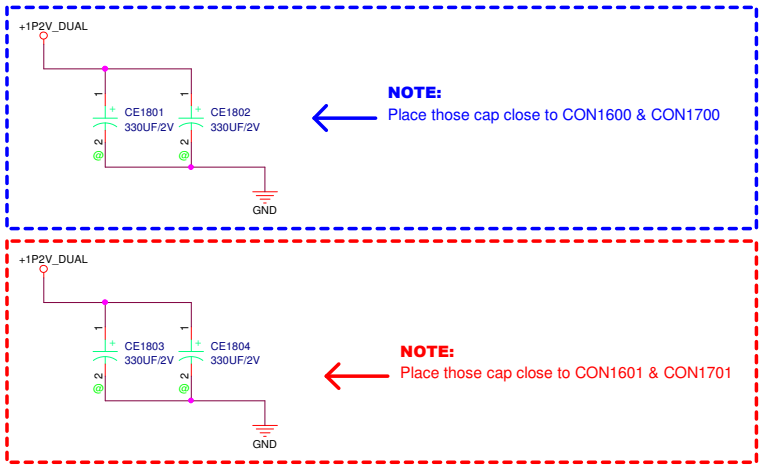
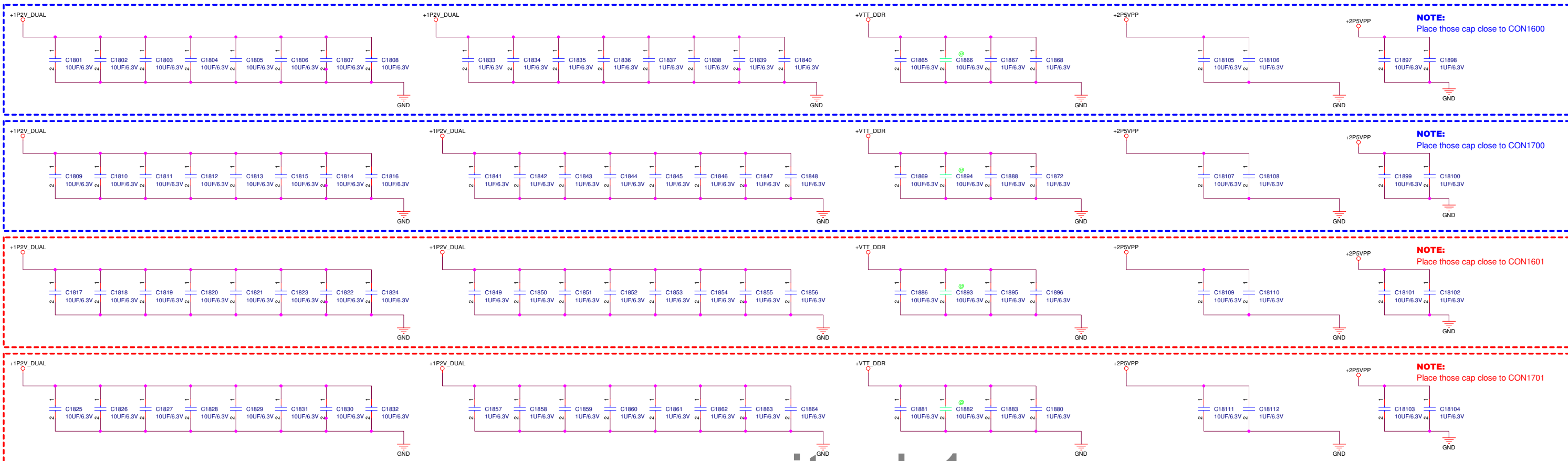




PEGATRON		Title :HDD REPEATER	
Pegatron Corp.		Engineer: Kai_Shen	
Size B	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet	15 of 101



STATUS	SA2	SA1	SA0
CON1600	0	0	0
CON1601	0	0	1

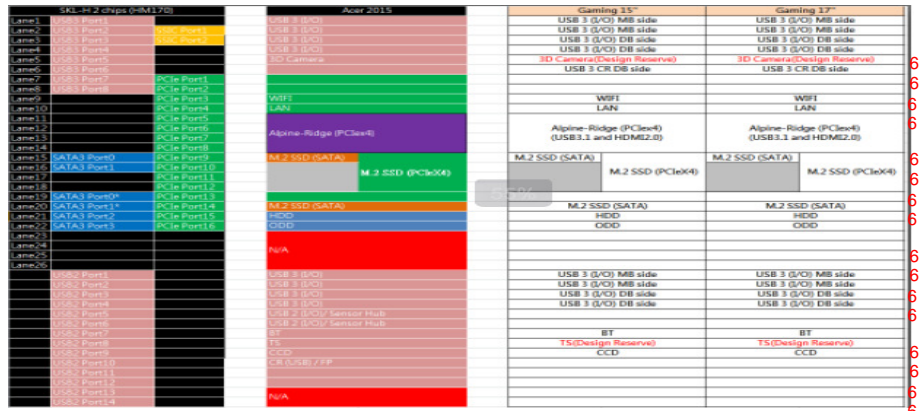


KBL-H PDG #564042, V0.9
Table 4-25. DDR4 SODIMM Power Plane Decoupling

DDR4 2 Channels SODIMM 2DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	32 x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	32 x 1µF (0402)	
		1 placeholder	2x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	2x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	2x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	8x 1µF (0402)	
	VPP	DRAM Side	4x 10µF (0603)	
		DRAM Side	4 x 1µF (0402)	
VDDSPD		Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0603)	

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NOTE:
PCH EDS 0.7



M.2 WiGi

M.2 WLAN

LAN E2400

Thunderbolt

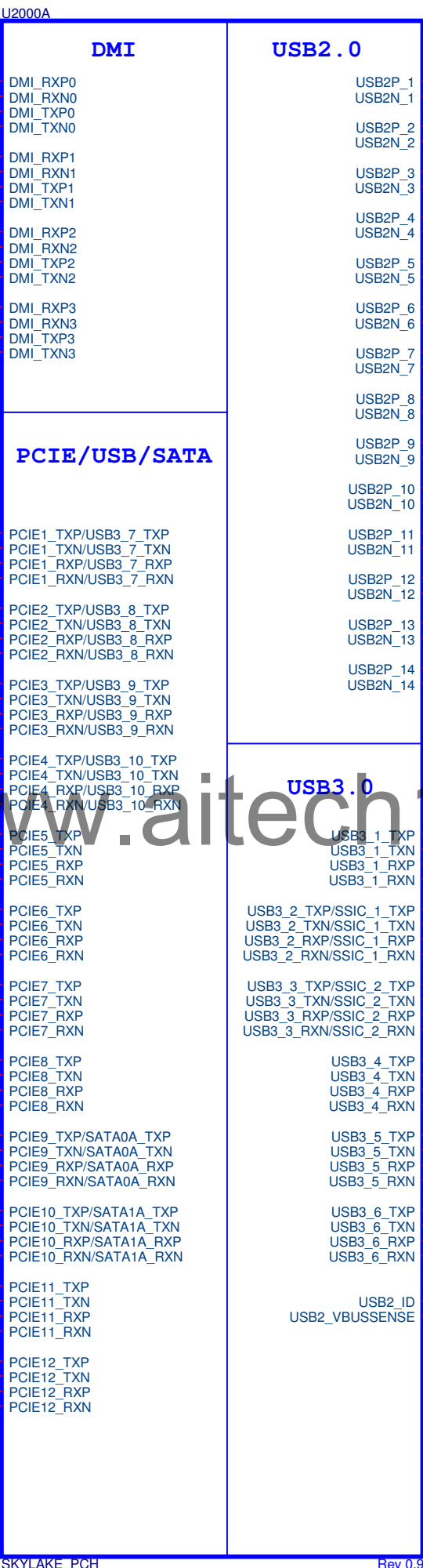
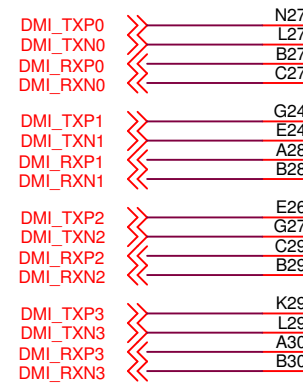
20160503 RFQ Kai
Change from 0.1uF to 0.22uF
follow Intel PDG

SATA Port1
(SSD)

SATA Port1
(SSD)

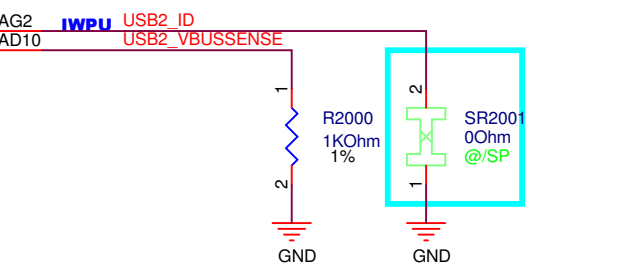
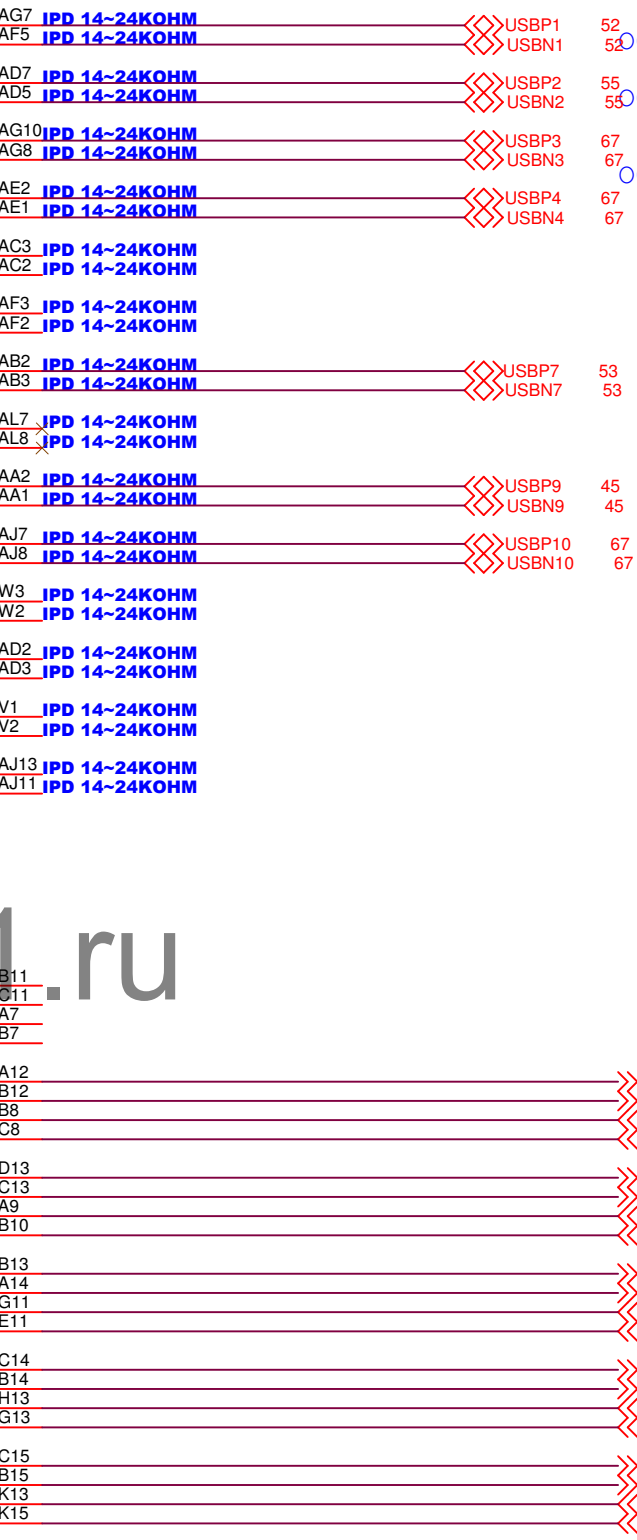
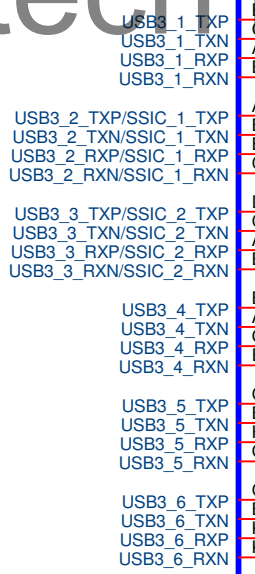
SATA Port1
(SSD)

SATA Port1
(SSD)



NOTE:
Lynx Point: USB2[0:13]
Sunrise Point PCH-H: USB2[1:14]

USB3.0



USB3.0 on-board

USB3.0 IO-board

M.2 BT

WEBCAM

CARD READER

USB3.0 on-board

USB3.0 IO-board

USB3.0 on-board

USB3.0 CARD

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_DMI/PCIE

Pegatron Corp. Engineer: Kai Shen

Size A3 Project Name P7RCR Rev R1.0

Date: Monday, October 17, 2016 Sheet 20 of 101

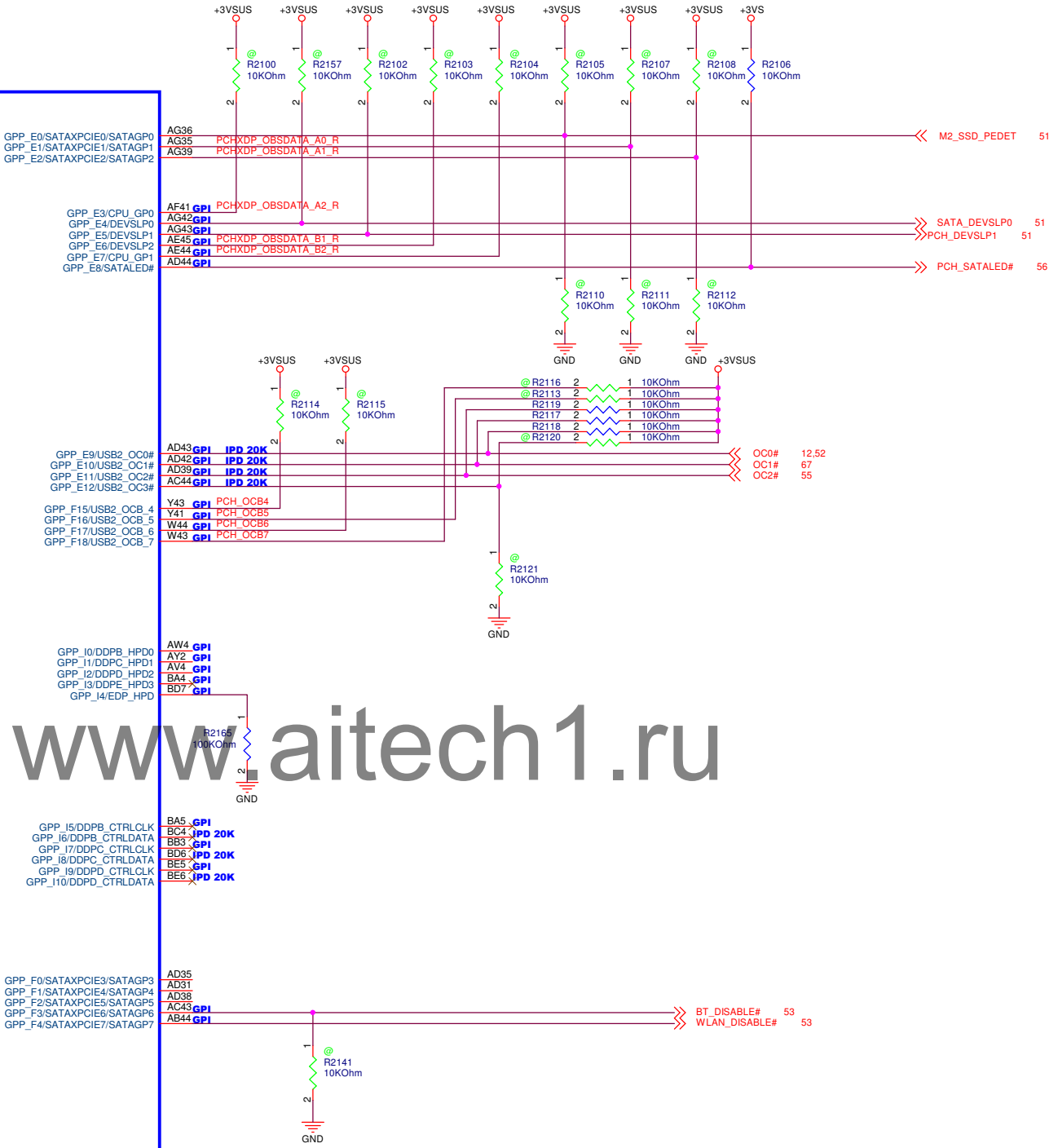
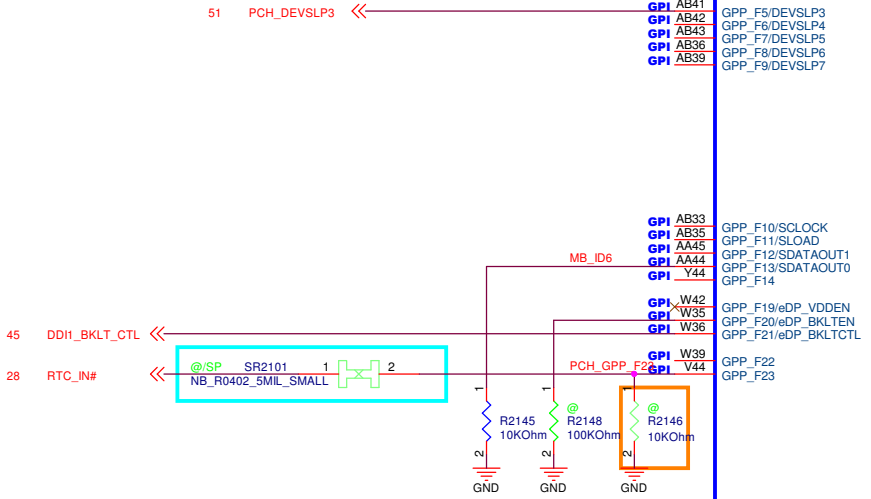
NOTE:
Check PU/PD

SATA Port2
(SSD)

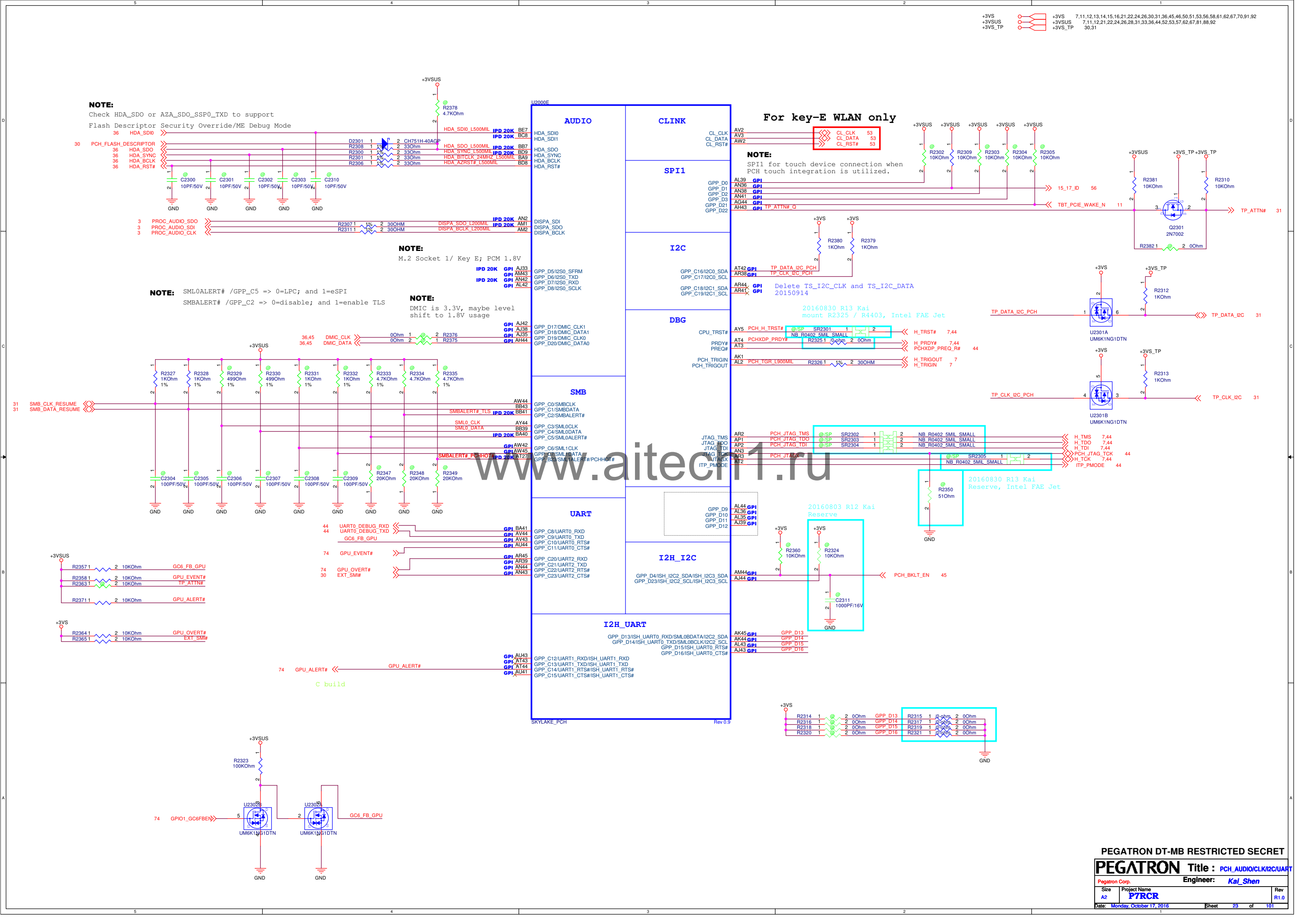
HDD

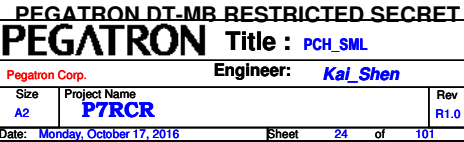
SATA Port3
(SSD)

STATUS	CTL1	CTL2	CTL3	ILIM_SEL
S0(CDP)	1	1	1	1
S3(CDP)	1	1	1	1
S4(DCP)	0	0	1	0
S5(DCP)	0	0	1	0

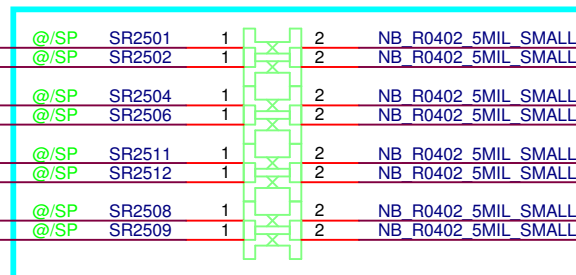


Pegatron Corp.		Engineer: Kai_Shen	
Size A2	Project Name P7RCR	Rev R1.0	
Date: Monday, October 17, 2016		Sheet 22 of 101	





7 CK_100M_BCK
7 CK_100M_BCK#
7 CK_24M_BCK
7 CK_24M_BCK#
7 CK_100M_PCIE
7 CK_100M_PCIE#
44 CK_100M_CPUXDP
44 CK_100M_CPUXDP#

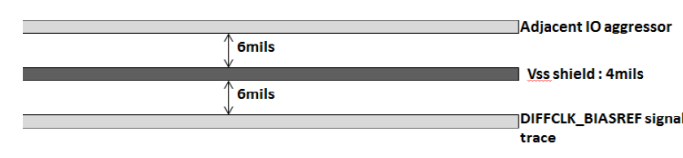
**NOTE:**

CRB: 2.71Kohm

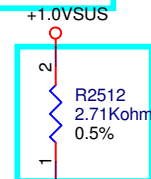
Refer to GND; NOT near switching noise; spacing 3x

Add a GND shield(Width>4 mils)

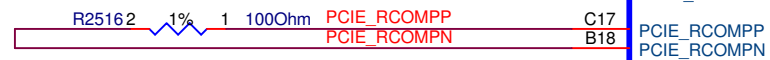
between XCLK_BIASREF and adjacent IO signals



20160803 R20 Kai
change for Intel spec
2.7k-ohm/1% to 2.71k-ohm/0.5%



XCLK_BIASREF



AN17 TP1
AR19 TP2
N29 RSVD3
N31 RSVD4
P24 RSVD5
P27 RSVD6
P29 RSVD7
P31 RSVD8
R24 RSVD9
R27 RSVD10
U13 RSVD11
W13 RSVD12
AB13 RSVD13
AE17 RSVD14
AF17 RSVD15
AG14 RSVD16
AG15 RSVD17
AN29 RSVD18
AR22 RSVD19
BD1 RSVD20
BE2 RSVD21

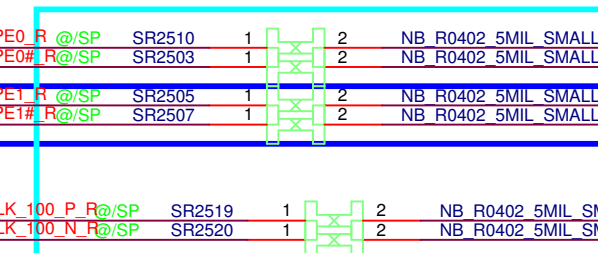
U2000C

CLOCK

XCLK_BIASREF
PCIE_RCOMP
PCIE_RCOMP_N

CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUPCIBCLK_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_ITPXDP_P
CLKOUT_ITPXDP_N
CLKOUT_PCIE_P0
CLKOUT_PCIE_N0
CLKOUT_PCIE_P1
CLKOUT_PCIE_N1
CLKOUT_PCIE_P2
CLKOUT_PCIE_N2
CLKOUT_PCIE_P3
CLKOUT_PCIE_N3
CLKOUT_PCIE_P4
CLKOUT_PCIE_N4
CLKOUT_PCIE_P5
CLKOUT_PCIE_N5
CLKOUT_PCIE_P6
CLKOUT_PCIE_N6
CLKOUT_PCIE_P7
CLKOUT_PCIE_N7
CLKOUT_PCIE_P8
CLKOUT_PCIE_N8
CLKOUT_PCIE_P9
CLKOUT_PCIE_N9
CLKOUT_PCIE_P10
CLKOUT_PCIE_N10
CLKOUT_PCIE_P11
CLKOUT_PCIE_N11
CLKOUT_PCIE_P12
CLKOUT_PCIE_N12
CLKOUT_PCIE_P13
CLKOUT_PCIE_N13
CLKOUT_PCIE_P14
CLKOUT_PCIE_N14
CLKOUT_PCIE_P15
CLKOUT_PCIE_N15

N8 CK_100M_PE0_R @/SP SR2510
N7 CK_100M_PE0#_R @/SP SR2503
L5 CK_100M_PE1_R @/SP SR2505
L7 CK_100M_PE1#_R @/SP SR2507
F2 TBT_REFCLK_100_P_R @/SP SR2519
D3 TBT_REFCLK_100_N_R @/SP SR2520
W11 CK_100M_PE8_R @/SP SR2513
W10 CK_100M_PE8#_R @/SP SR2514
N2 PCIE_CLK_P_GPU_R @/SP SR2515
N3 PCIE_CLK_N_GPU_R @/SP SR2516
P2 CK_100M_LAN_R @/SP SR2517
P3 CK_100M_LAN#_R @/SP SR2518



CK_100M_PE0 53
CK_100M_PE0# 53
CK_100M_PE1 53
CK_100M_PE1# 53
TBT_REFCLK_100_P 1
TBT_REFCLK_100_N 1
CK_100M_PE8 51
CK_100M_PE8# 51
PCIE_CLK_P_GPU 70
PCIE_CLK_N_GPU 70
CK_100M_LAN 33
CK_100M_LAN# 33

M2 WLAN

M2 WiGi

Thunderbolt

M2 SSD

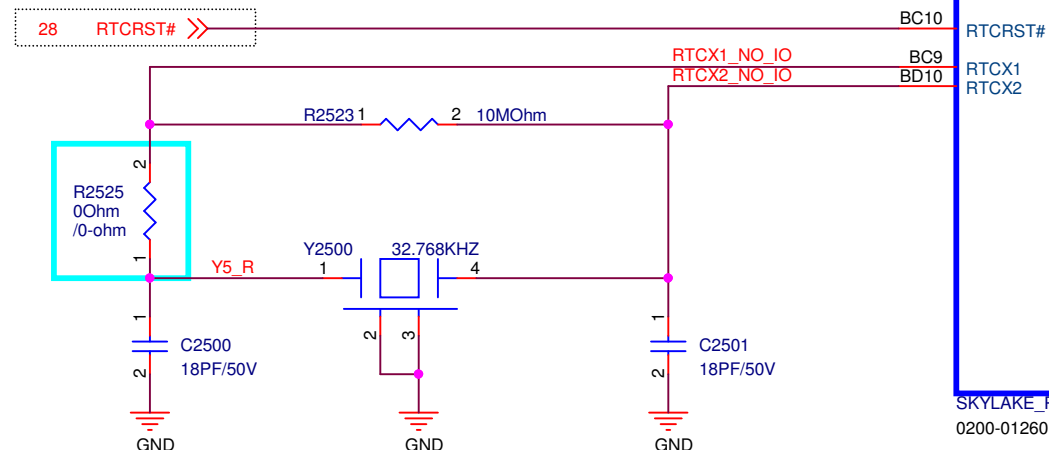
GPU

LAN

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NOTE:

RVP 10 CRB 0.5 use 30.1K ohm on RTCRST#

**NOTE:**

Be careful on RTC crystal(routing and test point) on AiO

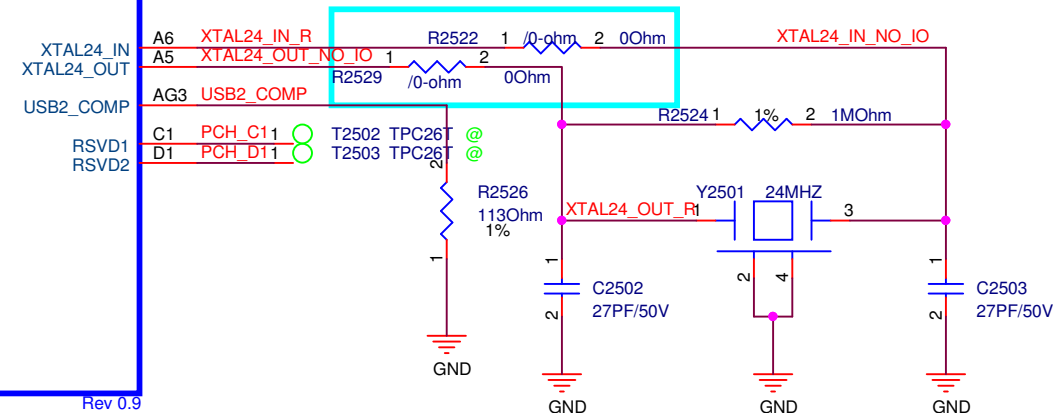
Instead of DIP to SMD if possible

Reduce trace length mismatch between RTCX1 & RTCX2

Do NOT route High Speed or GPIO(tie to header/connector) near X'tal region

NOTE:

Check 24MHz crystal spec



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH_CLOCK

Pegatron Corp. Engineer: Kai_Shen

Size A3	Project Name P7RCR	Rev R1.0
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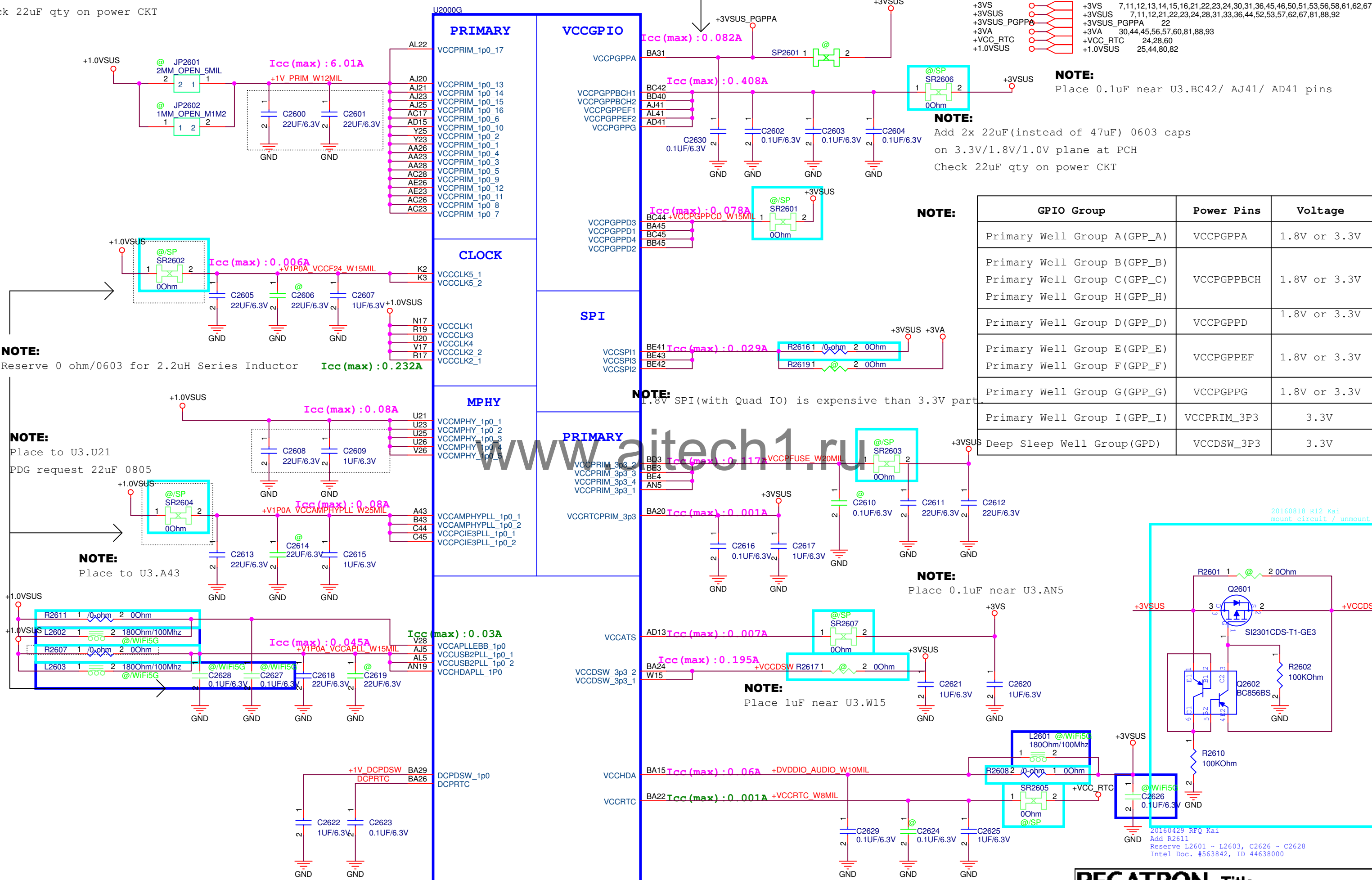
Date: Monday, October 17, 2016 Sheet 25 of 101

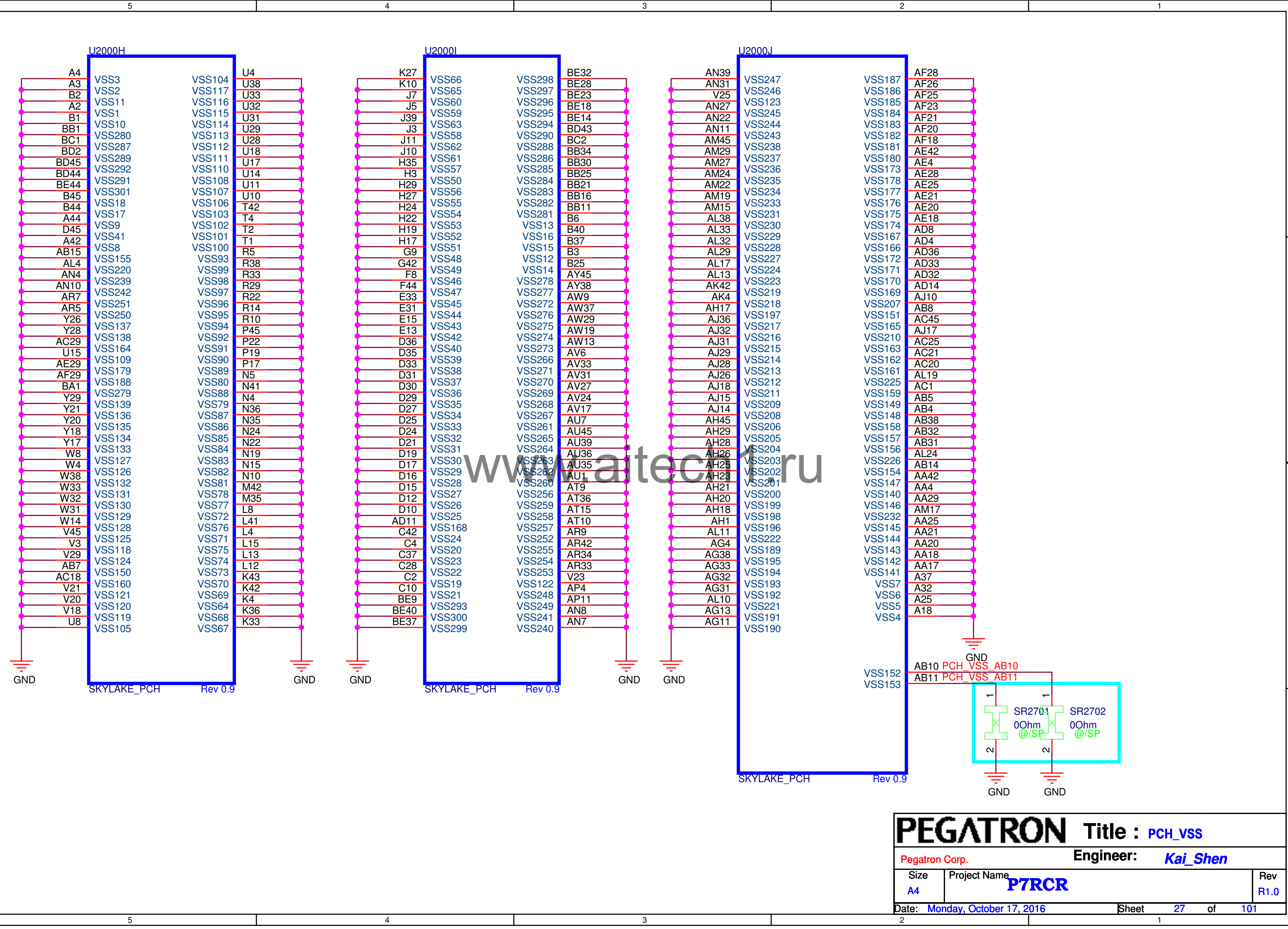
NOTE:

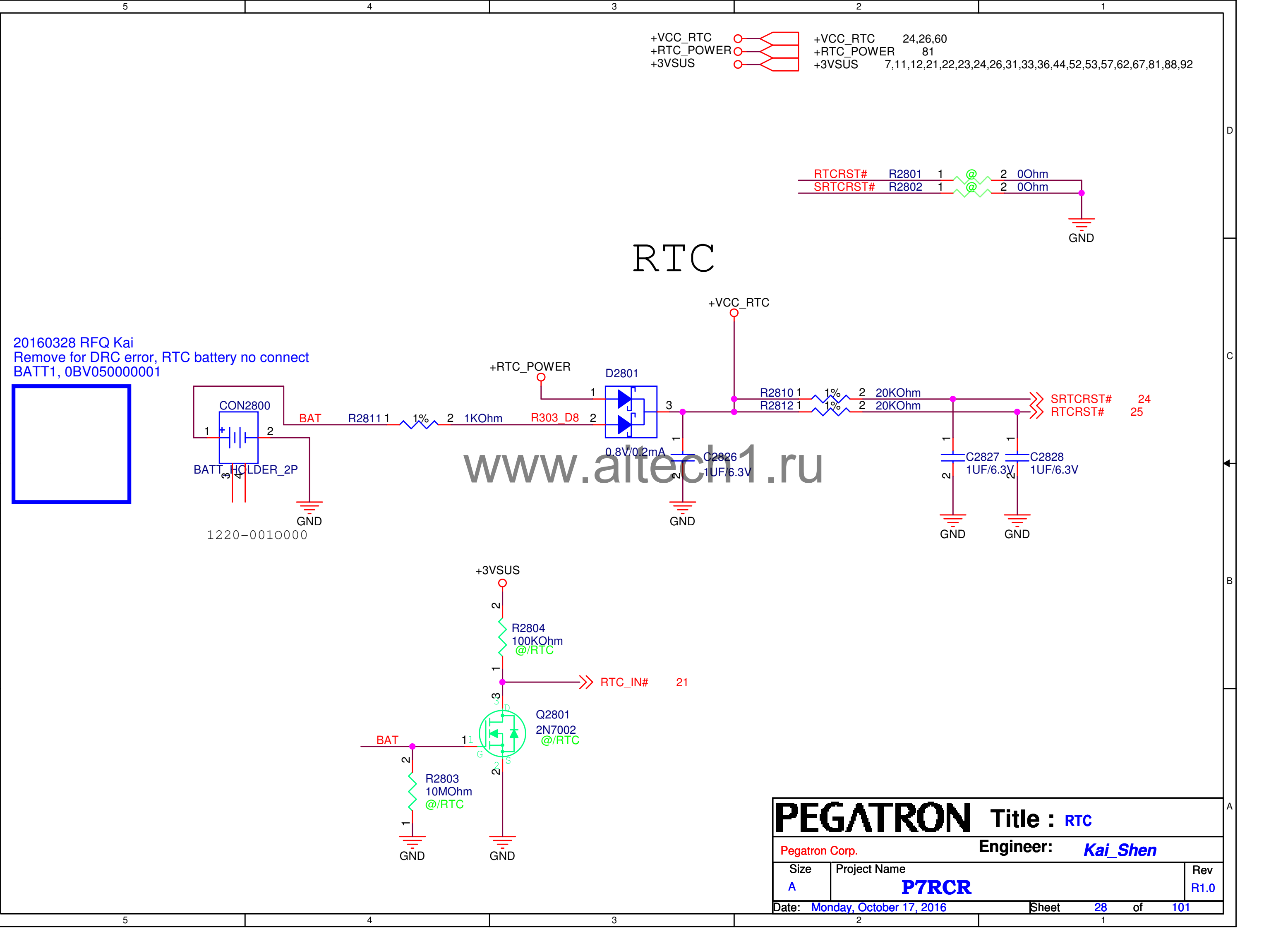
Add 2x 22uF(instead of 47uF) 0603 caps
on 3.3V/1.8V/1.0V plane at PCH
Check 22uF qty on power CKT

NOTE:

Check real GPIO implementation to decide VccGPIO rail is 3.3V or 1.8V



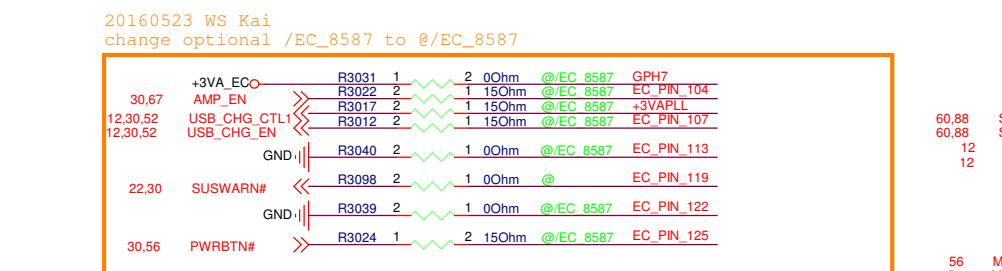
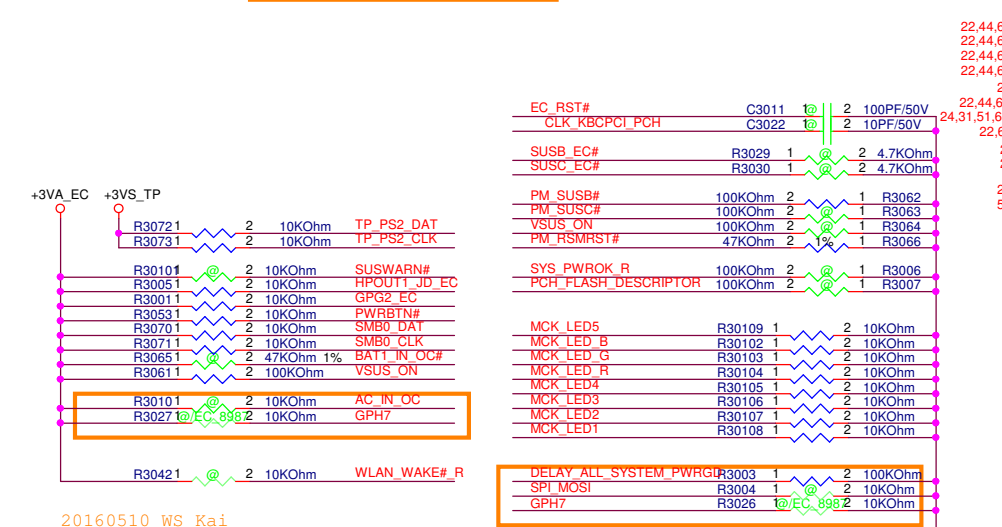
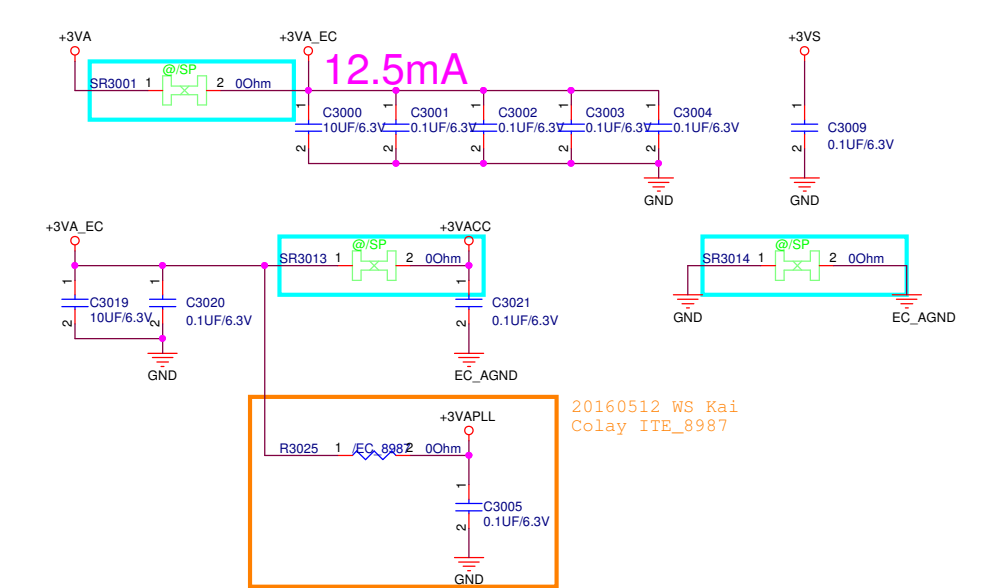




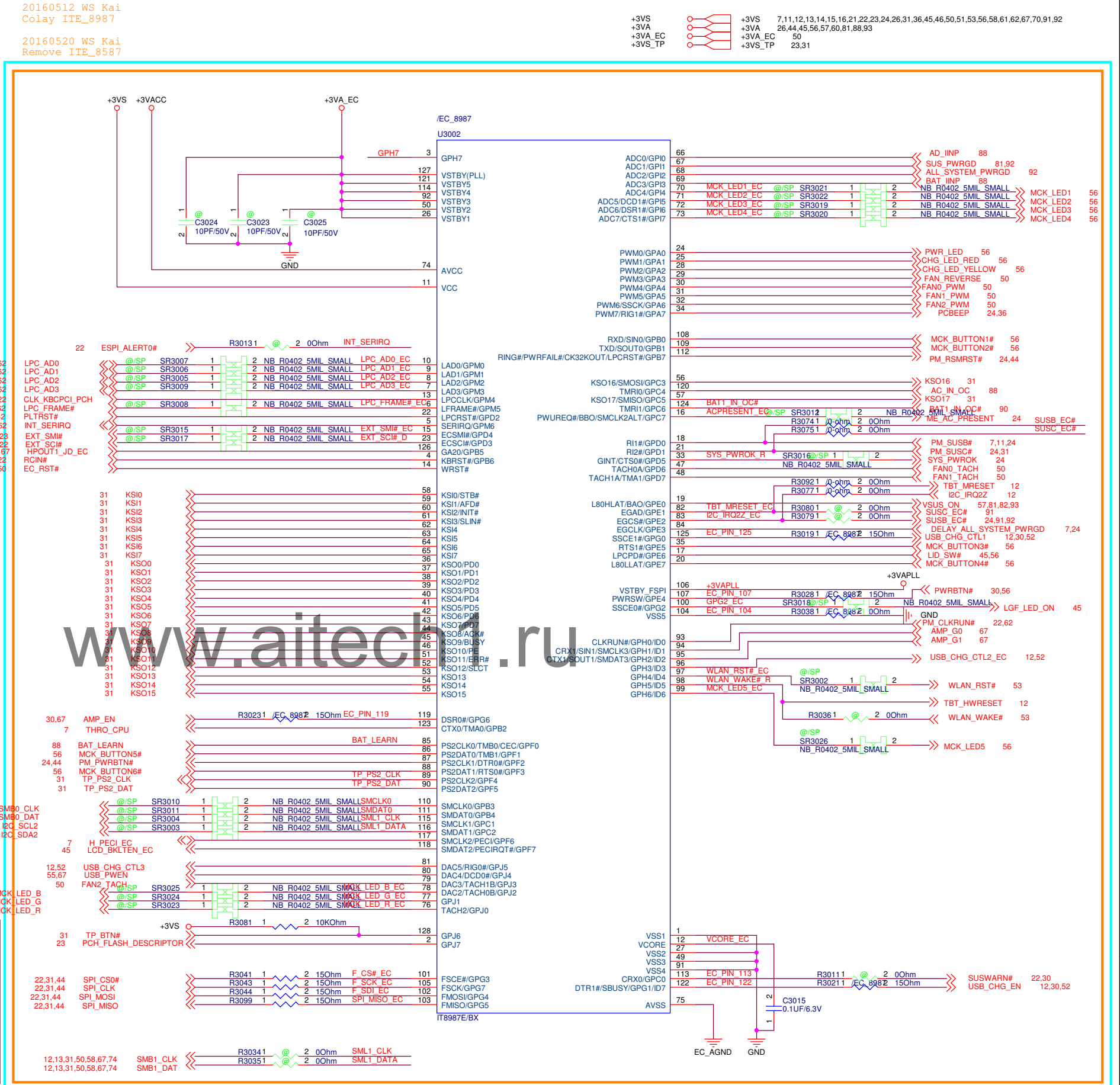
+VCC_RTC	24,26,60
+RTC_POWER	81
+3VSUS	7,11,12,21,22,23,24,26,31,33,36,44,52,53,57,62,67,81,88,92

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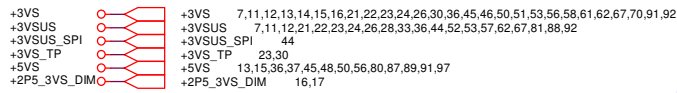
PEGATRON		Title :	DDR3 TERMINATION A&B
Pegatron Corp.		Engineer:	Kai_Shen
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016	Sheet 29 of 101		



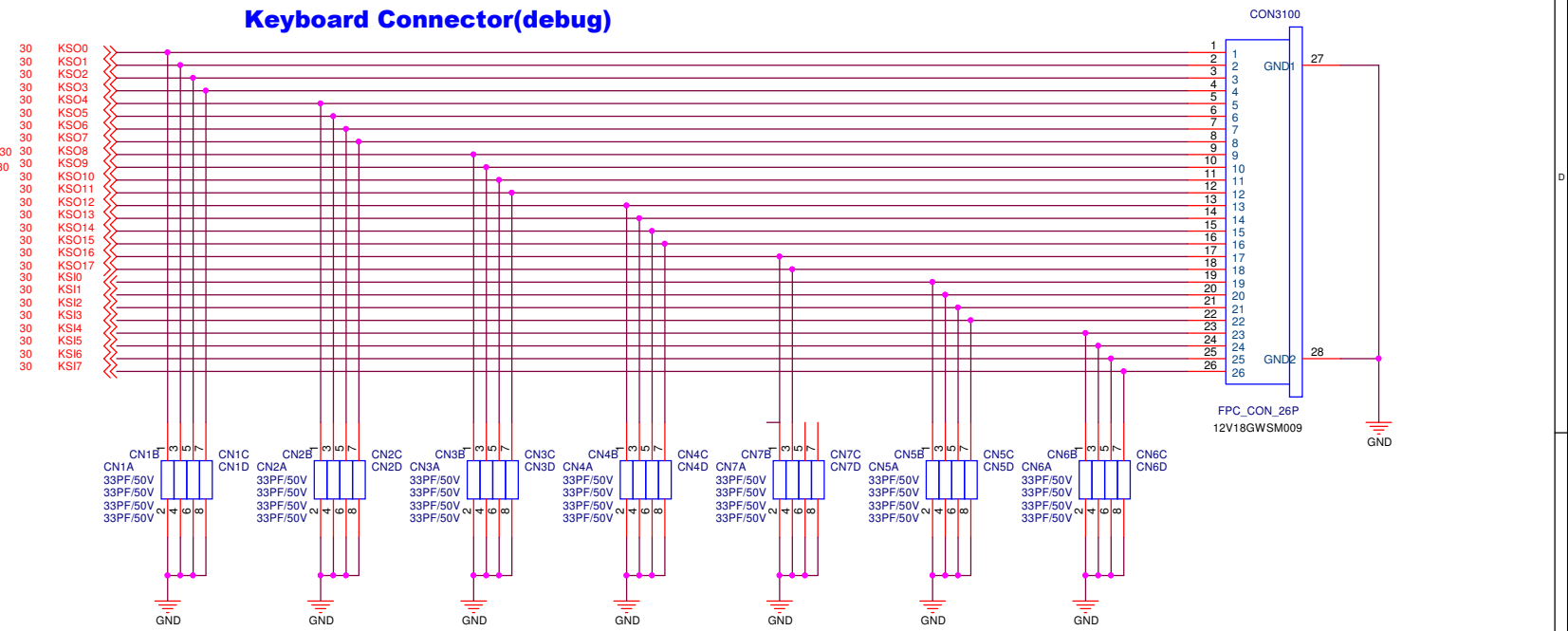
Pin	ITE8587	ITE8987	Note
3	VBAT	GPH7	VBAT → +3VA_EC
104	DSR0#/GPG6	VSS5	VSS → Gnd.
106	SSCE1#/VCEN/GPG0	VSTBY_FSPI	VSTBY_FSPI → +3VAPLL
107	DTR1#/SBUSY/GPG1/ID7	PWRSW/GPE4	N/A
113	VSS5	CRX0/GPC0	VSS → Gnd.
119	CRX0/GPC0	DSR0#/GPG6	N/A
122	VSS6	DTR1#/SBUSY/GPG1/ID7	VSS → Gnd.
125	PWRSW/GPE4	SSCE1#/GPG0	N/A



TOUCH PAD

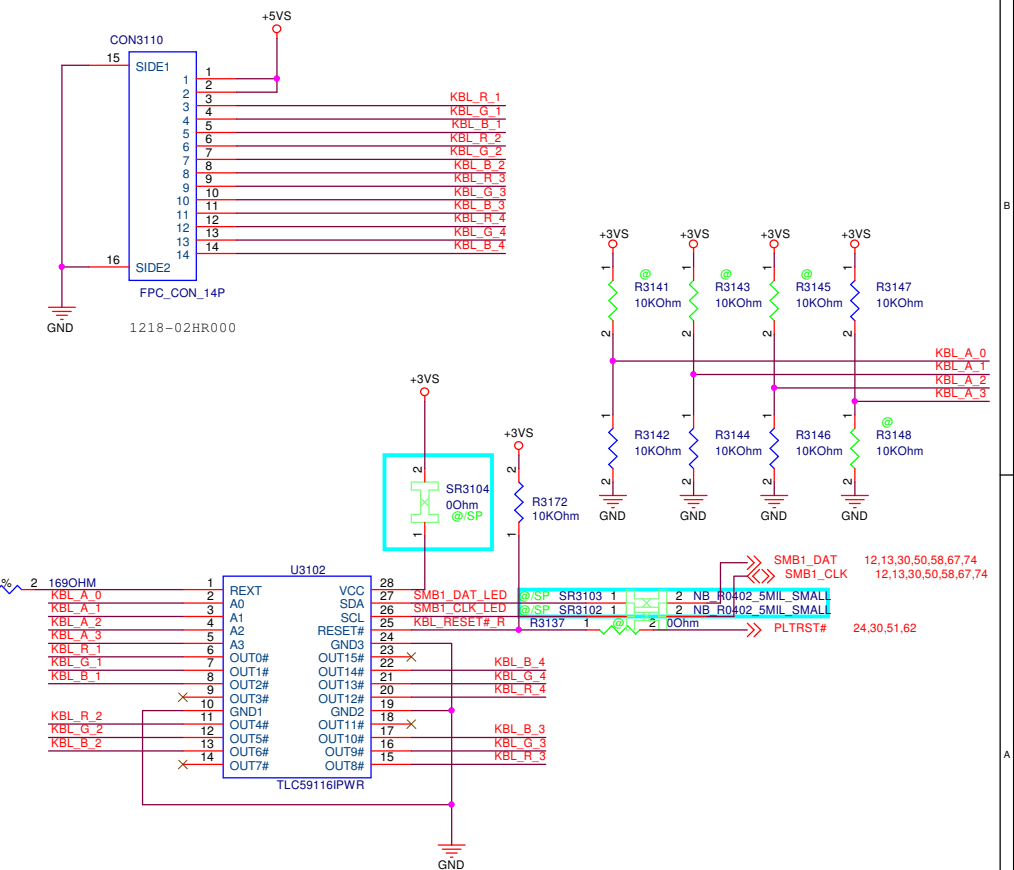


Keyboard Connector(debug)

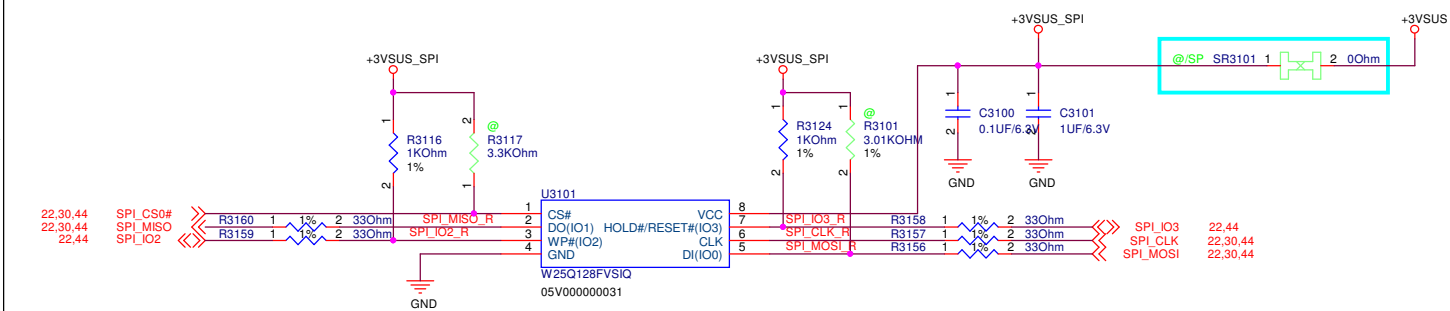


www.aitech1.ru

KB (Backlight)



SPI ROM (Quad I/O Supported)

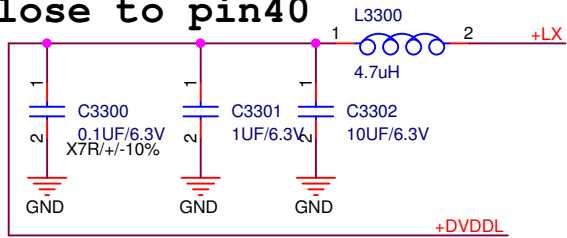


www.aitech1.ru

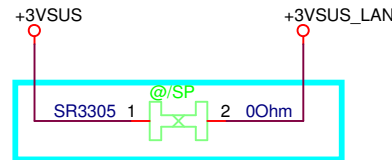
PEGATRON		Title :	DDR3 TERMINATION A&B
Pegatron Corp.		Engineer:	Kai_Shen
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016	Sheet 32 of 101		

L3300, C3300, C3301, C3302

Close to pin40



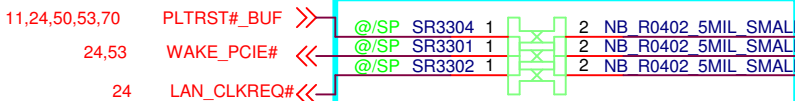
0.2A



+3VSUS 7,11,12,21,22,23,24,26,28,31,36,44,52,53,57,62,67,81,88,92

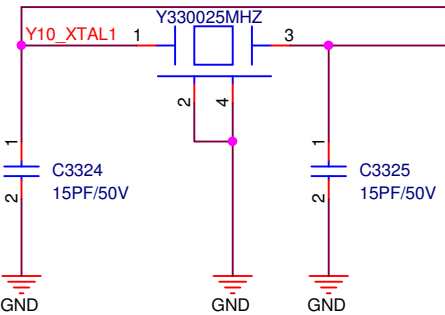


If AVDDL/DVDDL comes from internal SWR: mount L3302;
If AVDDL/DVDDL comes from internal LDO: no mout L3302



11,24,50,53,70
24,53
24

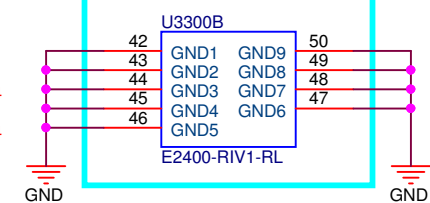
PLTRST#_BUF
WAKE_PCIE#
LAN_CLKREQ#



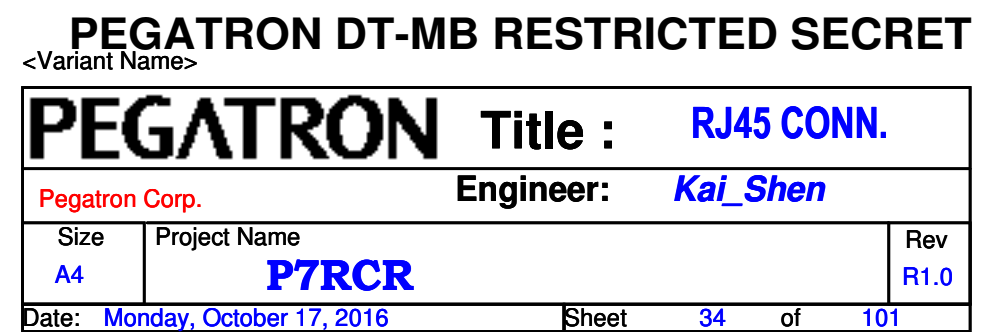
C3324 15PF/50V
C3325 15PF/50V

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LAN_MDIO_P
LAN_MDIO_N
LAN_MDIO_P
LAN_MDIO_N



20160817 R12 Kai
change E2400 to E2500
change 02V3T0000010 to 02V3T0000012
20161006 R14 Kai
change LAN back to E2400



5 4 3 2 1

D

C

B

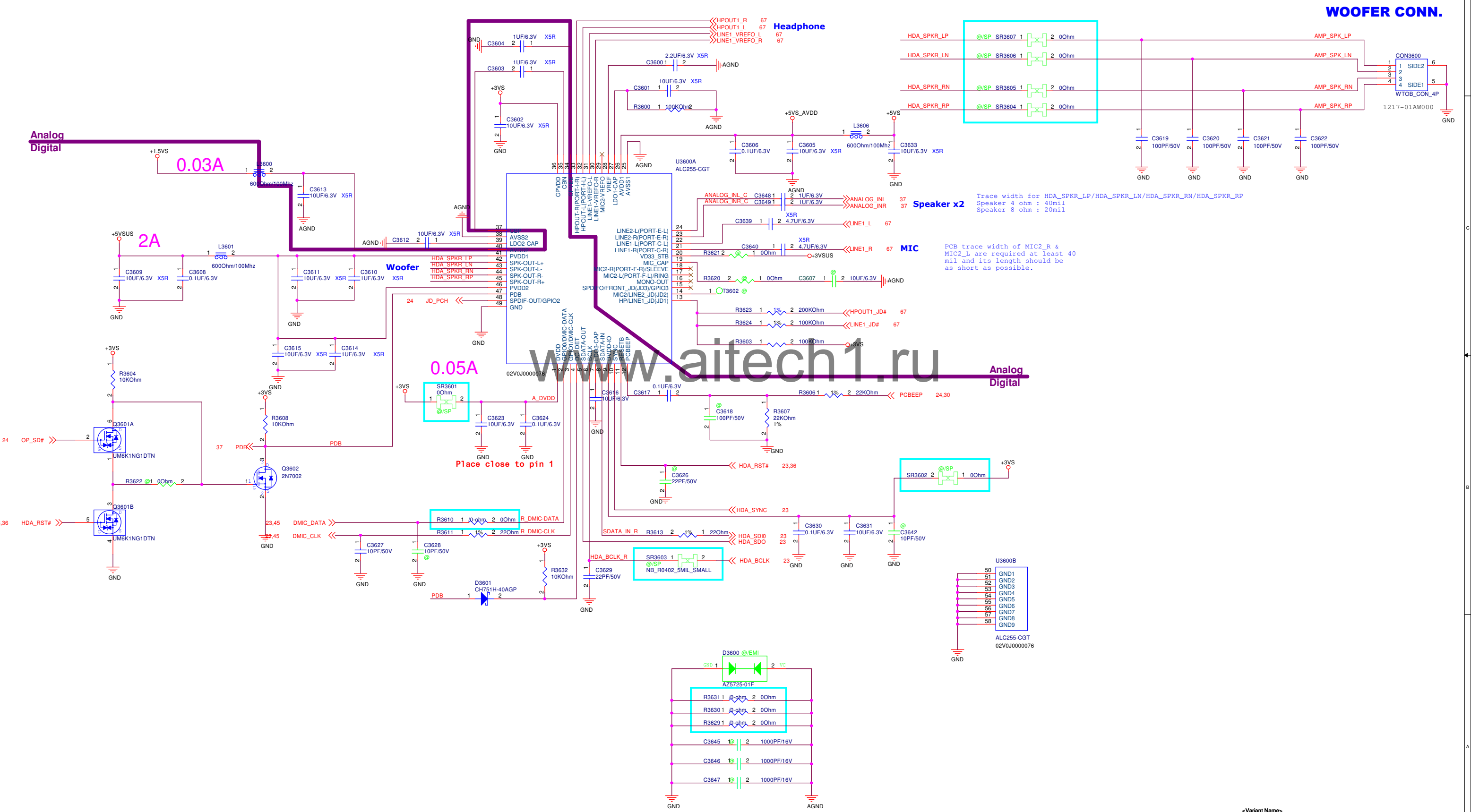
A

www.aitech1.ru

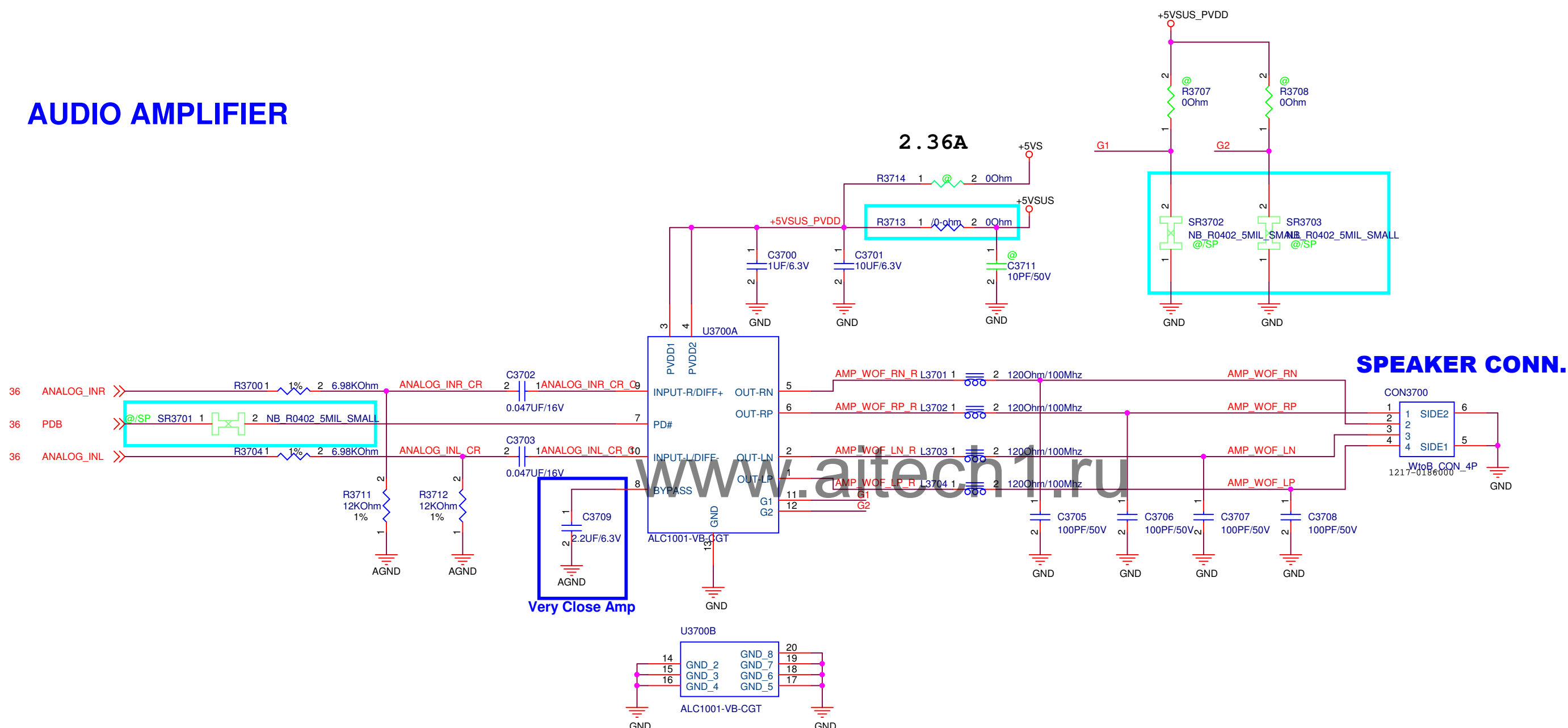
PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 35 of 101	

5 4 3 2 1

ALC255 CODEC



AUDIO AMPLIFIER



SPEAKER CONN.

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR	Rev R1.0	
Date: Monday, October 17, 2016		Sheet 38 of 101	

PEGATRON

Title : DDR3 TERMINATION A&B

Pegatron Corp. Engineer: Kai_Shen

Size	Project Name	Rev
A	P7RCR	R1.0

Date: Monday, October 17, 2016 Sheet 39 of 101

[illegible]

[illegible]

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 42 of 101	

www.aitech1.ru

PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 43 of 101	

The schematic diagram illustrates the debug connectors on the 1218-01AT000 board. Two connectors, CON4400 and CON4402, are shown. CON4400 is connected to LPC signals (LPC_AD0, LPC_AD1, LPC_AD2, LPC_AD3, LPC_FRAME#, CLK_KBCPCI_DEBUG) and a 3V supply. CON4402 is connected to UART0_DEBUG_TXD, UART0_DEBUG_RXD, SPI_CS0#, SPI_MISO, SPI_CLK, SPI_MOSI, and SPI_IO3. Both connectors are labeled 'FPC_CON_12P' and '1218-01AT000'.

Figure 1 illustrates the PCB footprint for the HRS/DF9C-31S-1V(22) connector. It includes three views: Top Side View, Bottom Side View, and a detailed view of the connector pins. The Top Side View shows a rectangular footprint with dimensions 0.1 and 0.2. The Bottom Side View shows the same footprint with dimensions 0.1 and 0.2. The detailed view shows the connector pins with dimensions 0.1 and 0.2.

BP_PWRGD_RST#
CPU_XDP_HOOK2
HOOK3_SPI_MOSI_VRM_PWRGD
HOOK6_ITP_PMODE_PLTRST_CPU#
FP_RST_DBR_N_CPUXDP

+1.0VSUS
+3VSUS
+VCCIO
+3VA

/Debug R4410 2.2KOhm
/Debug R4411 2.2KOhm
/Debug R4409 150Ohm 1%
/Debug R4412 1KOhm 1%

@ R4423 0Ohm
@ C4403 0.1UF/6.3V
/Debug C4401 0.1UF/6.3V
@ C4402 0.1UF/6.3V

@/SP SR4406 1 2 NB R0402 5MIL SMALL
R4414 1 2 1KOhm1%
R4415 1 2 0Ohm
R4416 1 2 1KOhm1%
R4417 1 2 0Ohm
R4418 1 2 1KOhm1%
@/SP SR4407 1 2 NB R0402 5MIL SMALL

ITP_PMODE 23
SPI_MOSI 22,30,31,44
PM_PWRBTN# 24,30
H_CFG0 7,44
VRM_PWRGD 24,80,92
PLTRST_CPU# 7,24
SYS_RESET# 24

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PCB FOOTPRINT

20160830 R13 Kai
Reserve R4427 / R4428 PH to 1V, Jay

R4427 1 @Debug2 510hm H_TDI
R4428 1 @Debug2 510hm H_TMS

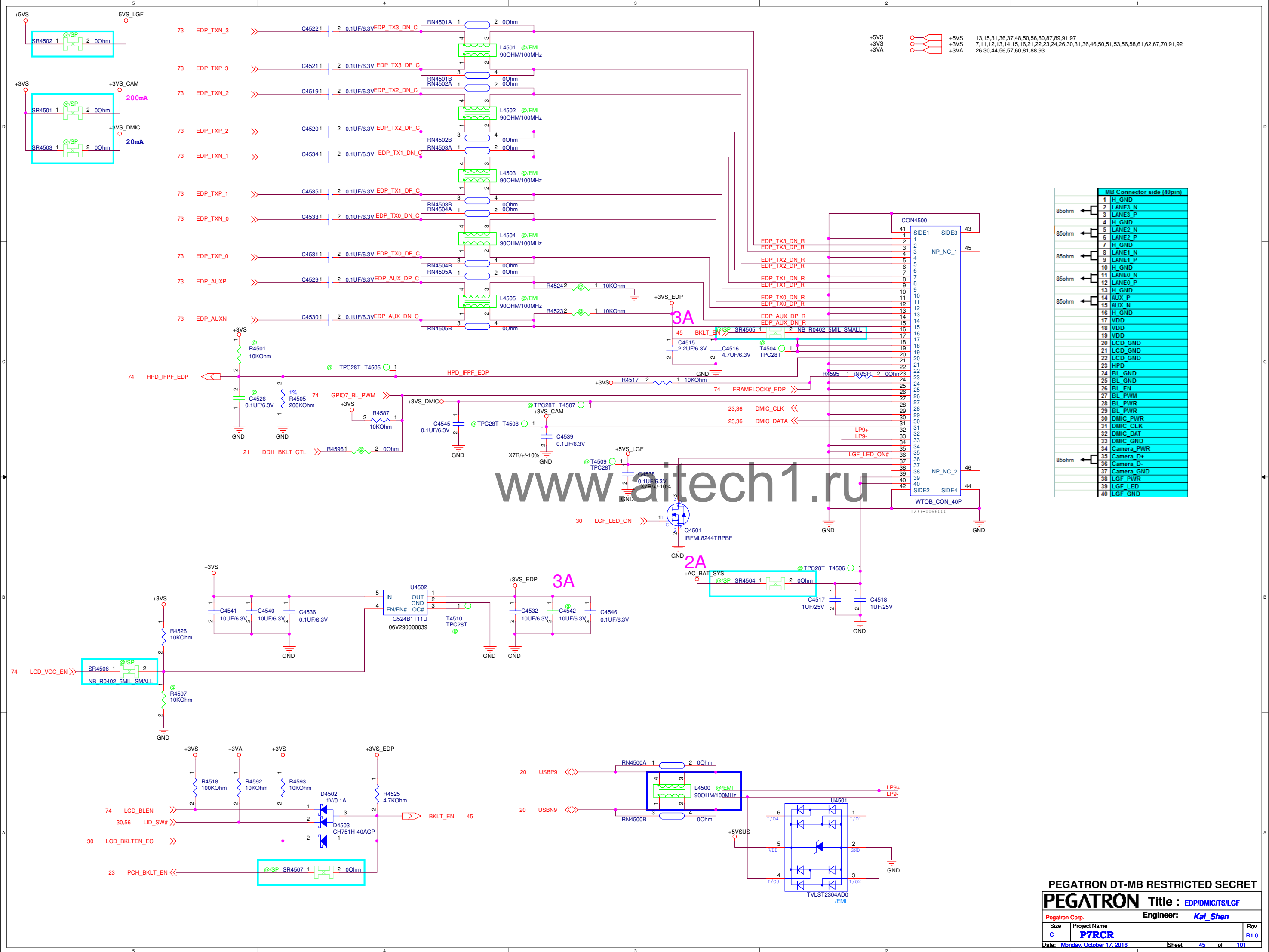
7 H_CFG17
7 H_CFG16
7 H_CFG8
7 H_CFG9
7 H_CFG10
7 H_CFG11
7 H_CFG19
7 H_CFG18
7 H_CFG12
7 H_CFG13
7 H_CFG14
7 H_CFG15
7,23 H_TDO
7,23 H_TRST#
7,23 H_TDI
7,23 H_TMS
22,31 SPI_I02
1KOhm 2
@Debug 1%
R4425
XDP1_PIN60
SR4410
NB_R0402 5MIL SMALL
@SP
GND
GND
GND

2 2
4 4
6 6
8 8
10 10
12 10
14 12
16 14
18 16
20 18
22 20
24 22
26 24
28 26
30 28
32 30
34 32
36 34
38 36
40 38
42 40
44 42
46 44
48 46
50 48
52 50
54 52
56 54
58 56
60 58
62 60
NP_NC1
NP_NC2
BioB_CON 60P

1 1
3 3
5 5
7 7
9 9
11 11
13 11
15 13
17 15
19 17
21 19
23 21
25 23
27 25
29 27
31 29
33 31
35 33
37 35
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41 39
43 41
45 43
47 45
49 47
51 49
53 51
55 53
57 55
59 57
61 59
63 61

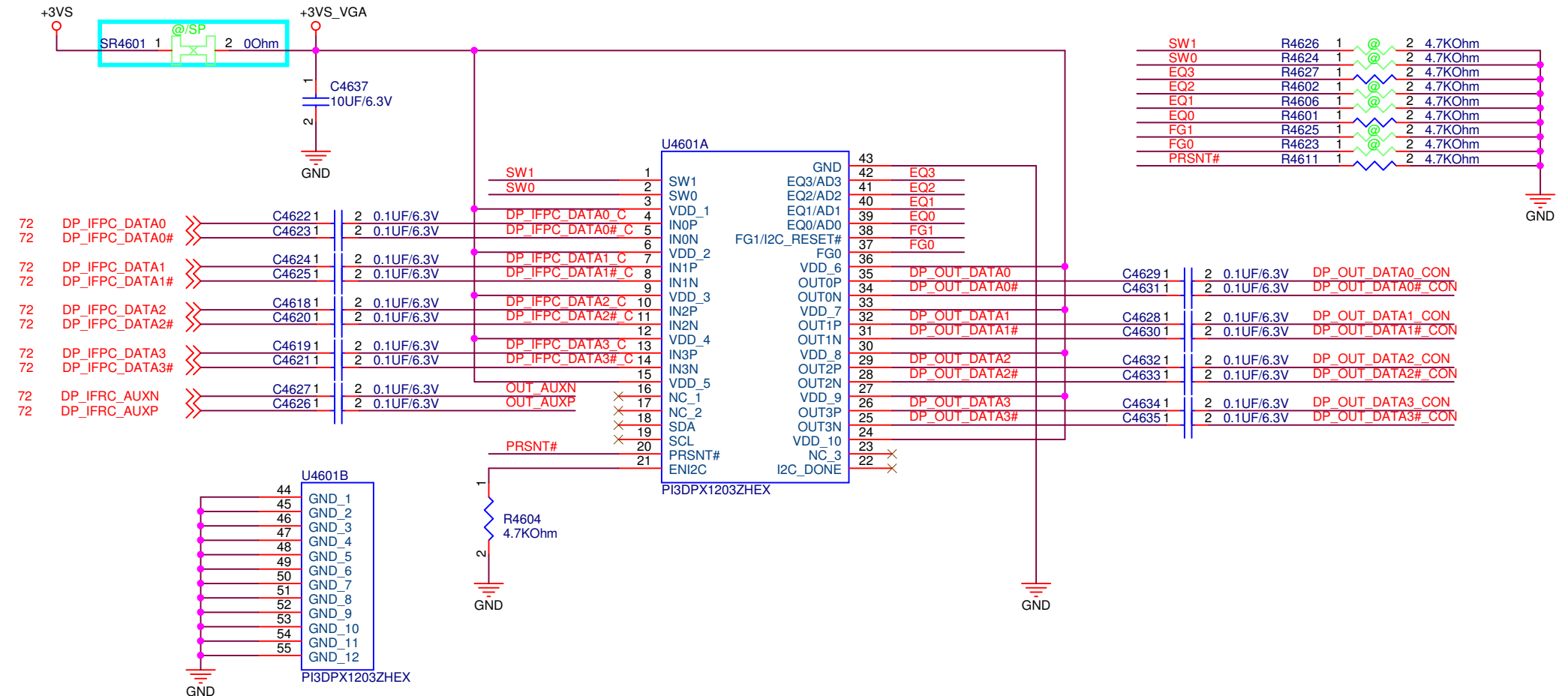
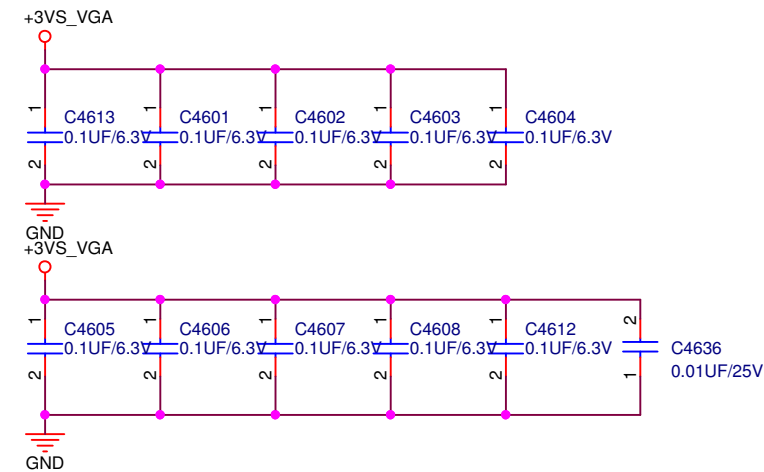
XDP_CPUDEBUG3
R44221 @Debug 2 1KOhm
H_CFG3 7,44
20160830 R13 Kai
mount R2325 / R4403, Intel FAE Jet
0Ohm 1 /Debug 2 R4403 1%
PCHXDP_PREQ_R# 23
H_PREQ# 7
H_PRDY# 7,23
H_CFG0 7,44
H_CFG1 7
H_CFG2 7
H_CFG3 7,44
H_BPM_N0 7
H_BPM_N1 7
NB_R0402 5MIL SMALL 1
SR4404@SP
NB_R0402 5MIL SMALL 1
SR4405@SP
H_CFG4 7
H_CFG5 7
H_CFG6 7
H_CFG7 7
CPU_XDP_HOOK0
BP_PWRGD_RST#
+CPU_VCC_OBS_CD
CPU_XDP_HOOK2
HOOK3_SPI_MOSI_VRM_PWRGD
SR4401@SP
O+1.0VSUS
R4404 1 2 1KOhm 1%
R4405 1 2 1KOhm 1%
R4406 1 2 1KOhm 1%
GPUPWRGD 7,24
VCCST_PG 7
PM_RSMRST# 24,30
SR4408 2 1 NB_R0402 5MIL SMALL
SR4409 2 1 NB_R0402 5MIL SMALL
SR4403 1 2 NB_R0402 5MIL SMALL
SMB_DATA_DEBUG 31
SMB_CLK_DEBUG 31
PCH_JTAG_TCK 23
H_TCK 7,23

PEGATRON		Title : DEBUG CON	
Pegatron Corp.		Engineer: Kai_Shen	
Size C	Project Name PTRCR	Rev R1	
Date: Monday, October 17, 2016		Sheet 44	of 101



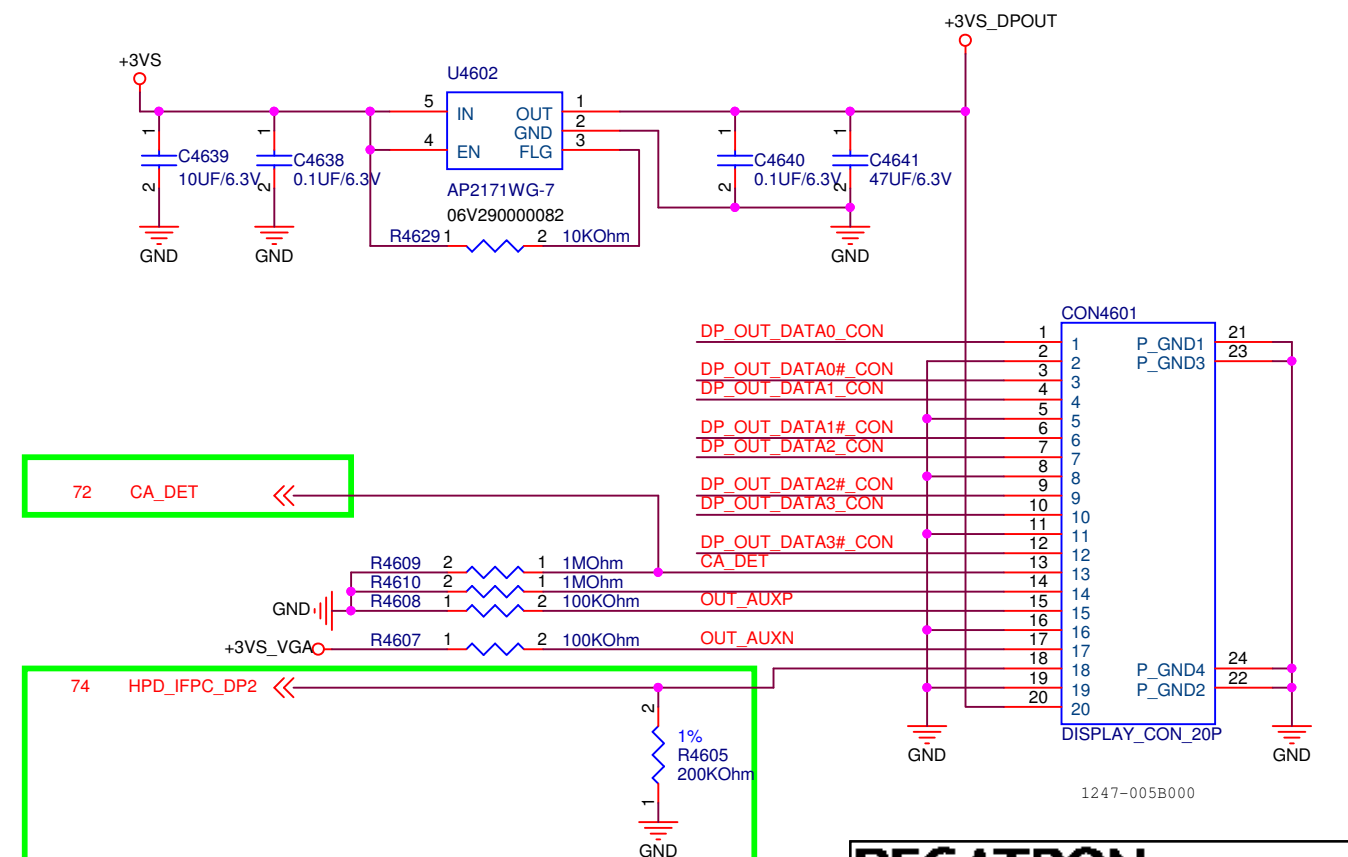
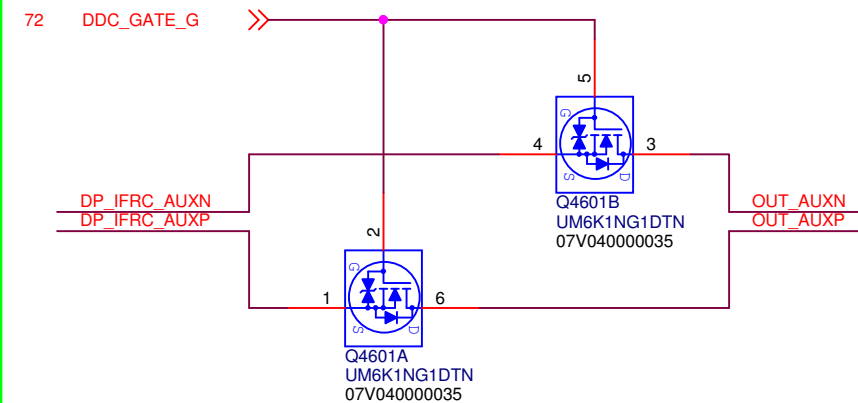
20160616 R1.1 Kai
change solution

20160621 R1.1 Kai
change U4601 to VX



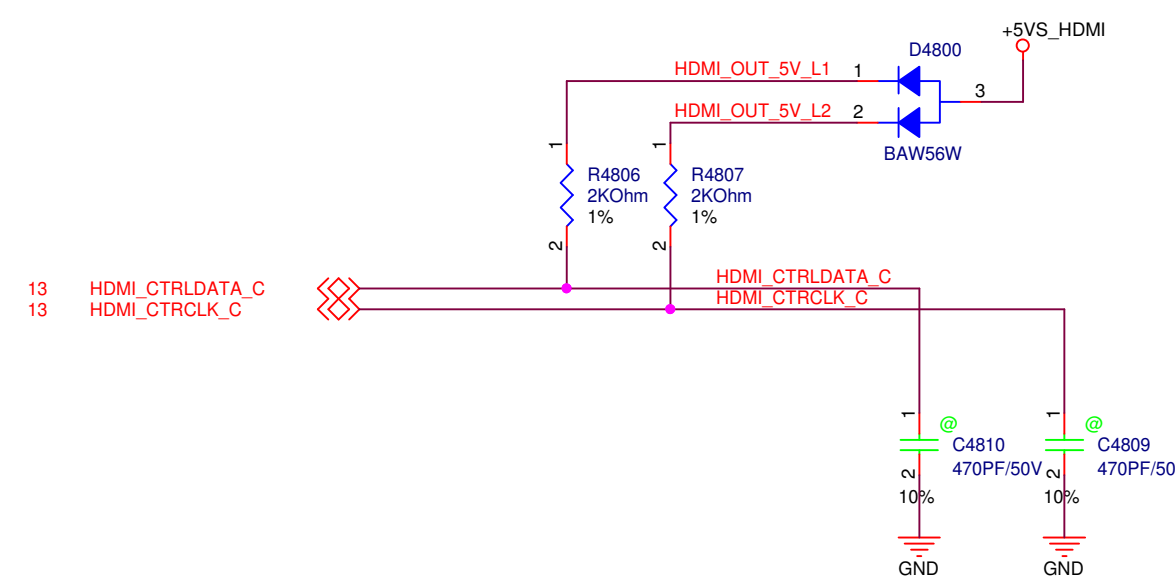
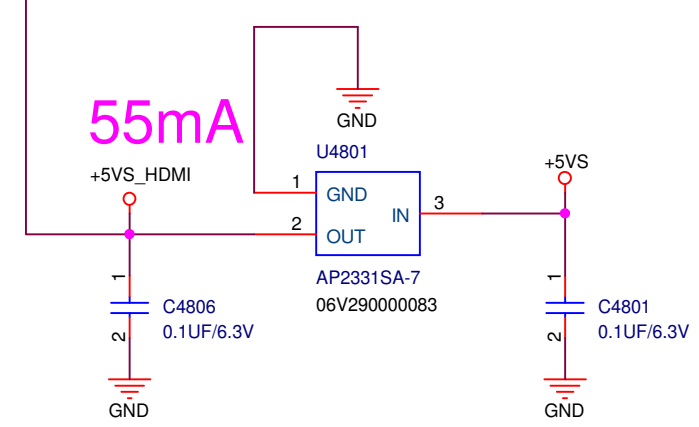
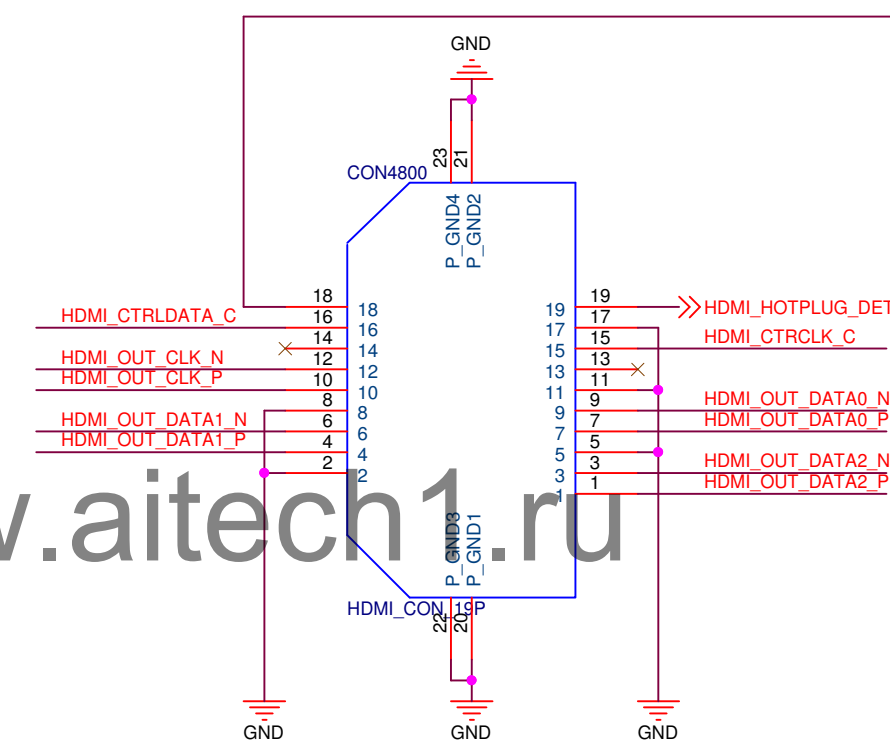
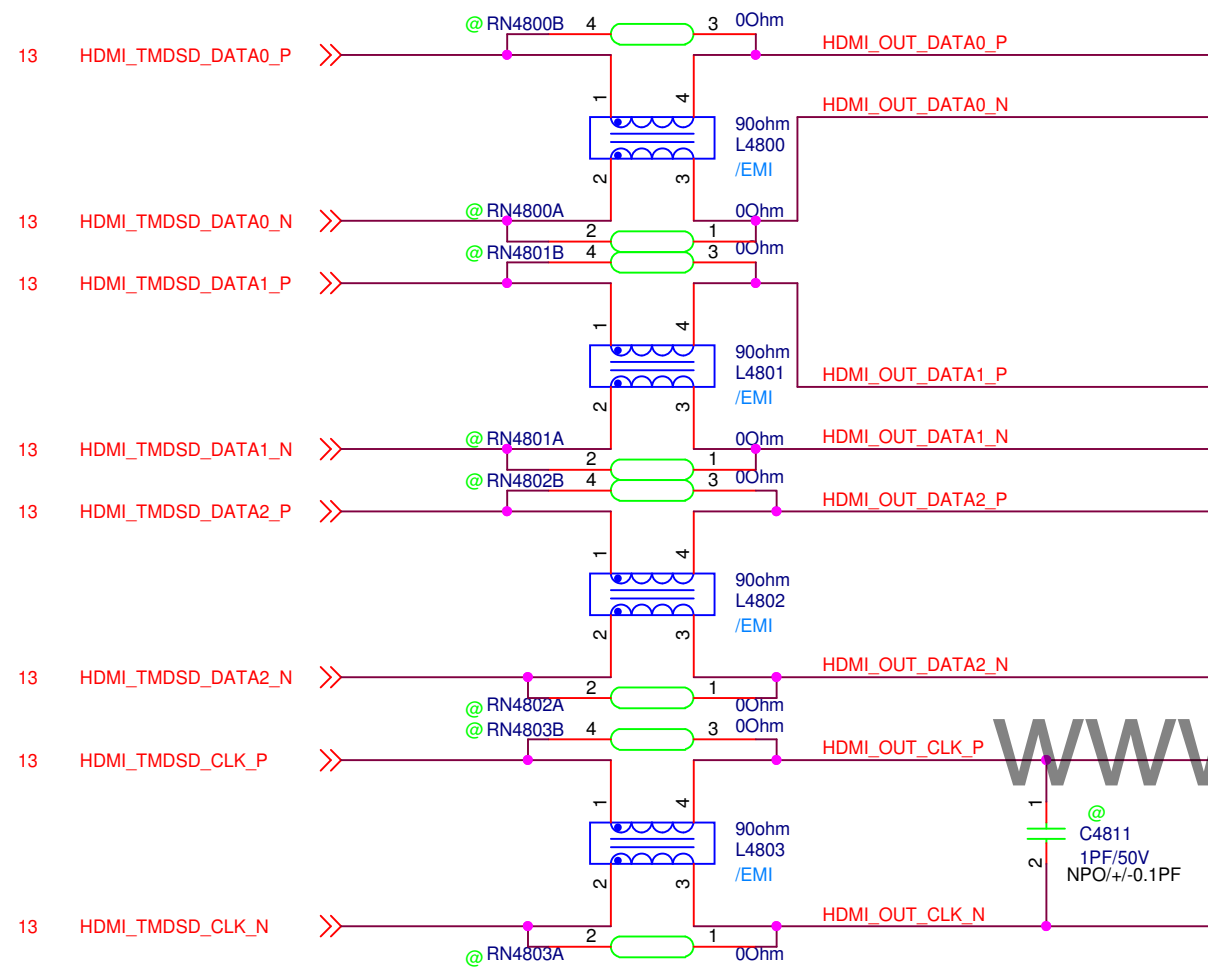
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20160622 R1.1 Kai
add DP++ circuit



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PEGATRON		Title : DDR3 TERMINATION A&B
Pegatron Corp.		Engineer: Kai_Shen
Size A	Project Name P7RCR	Rev R1.0
Date: Monday, October 17, 2016		Sheet 47 of 101

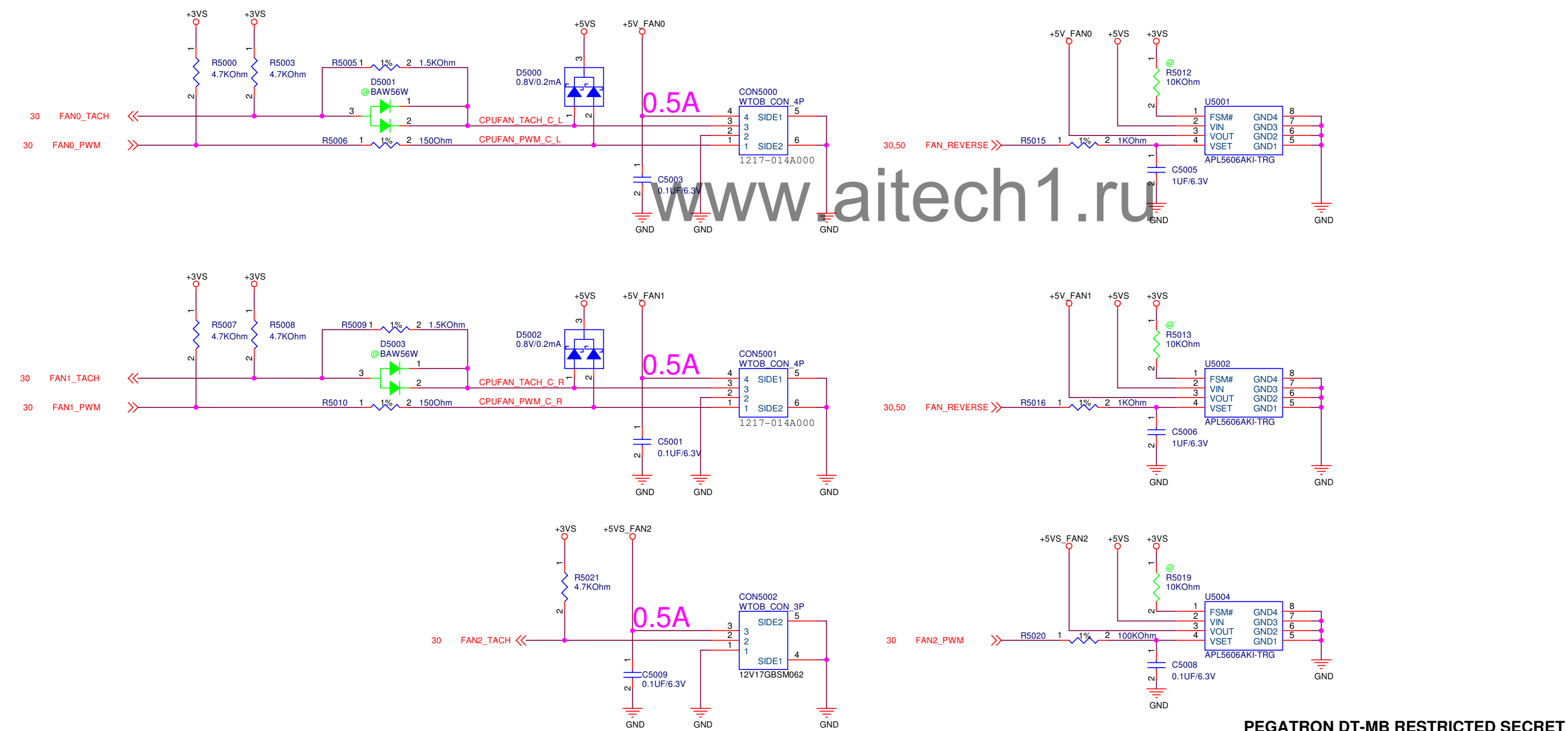
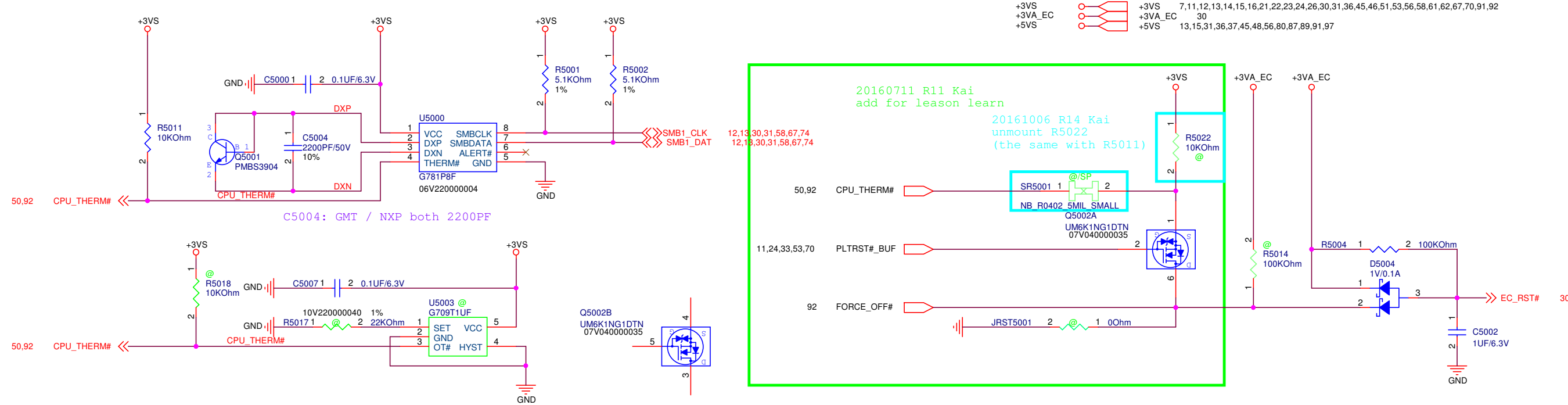


NOTE: HPDET status

High	Plugged
Low	Unplugged

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 49 of 101	



STATUS#, FAULT#, ILIM_LO, ILIM_HI Voltage: -0.3 to 7v.
STATUS#, FAULT# Continuous output sink current:25mA.
ILIM_LO, ILIM_HI Continuous output source current: Internally limited.

+3VSUS
+5VSUS
+5VSUS_CHARGING

+3VSUS 7,11,12,21,22,23,24,26,28,31,33,36,44,53,57,62,67,81,88,92
+5VSUS 12,36,37,45,55,56,57,67,81
+5VSUS_CHARGING 55

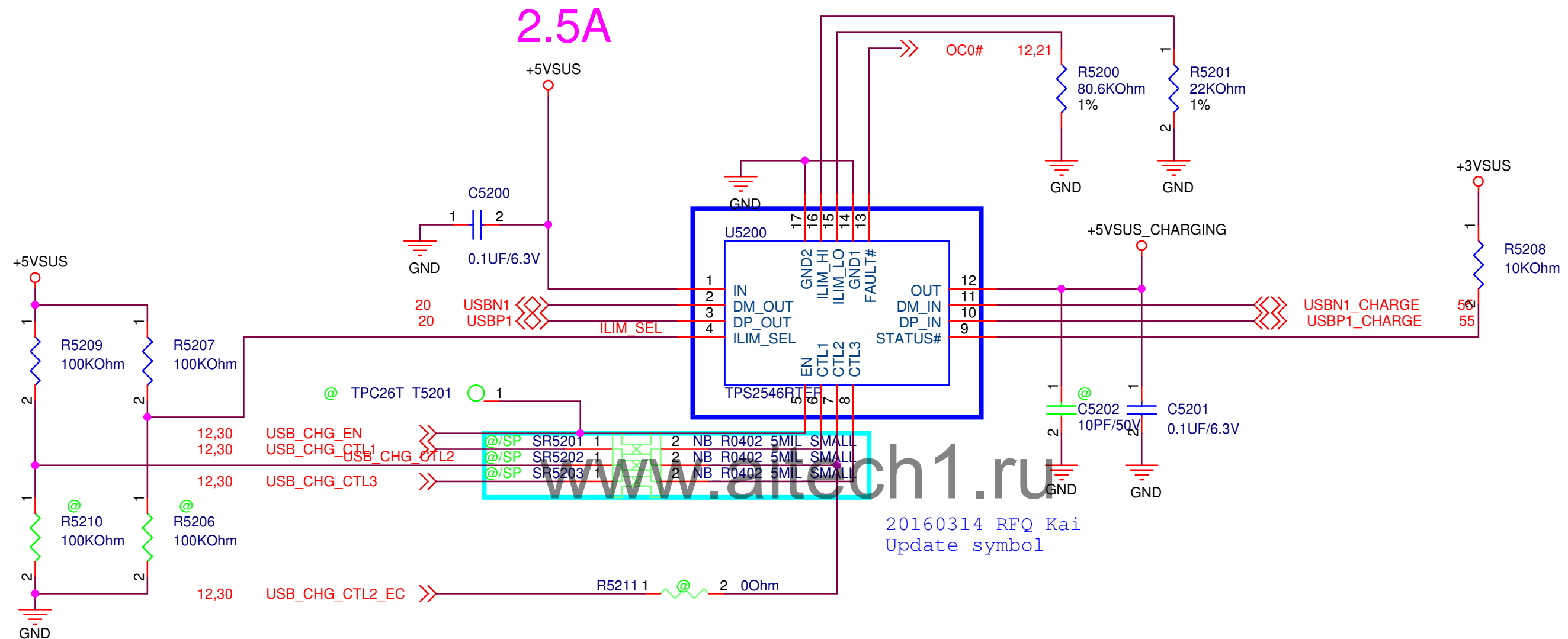


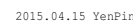
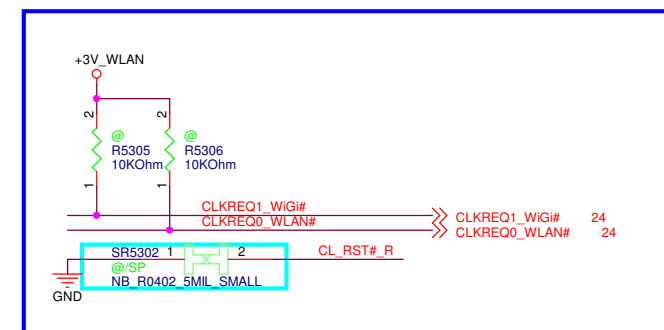
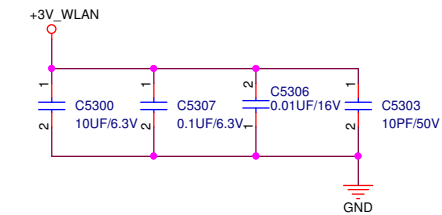
Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Status Output	Notice
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active

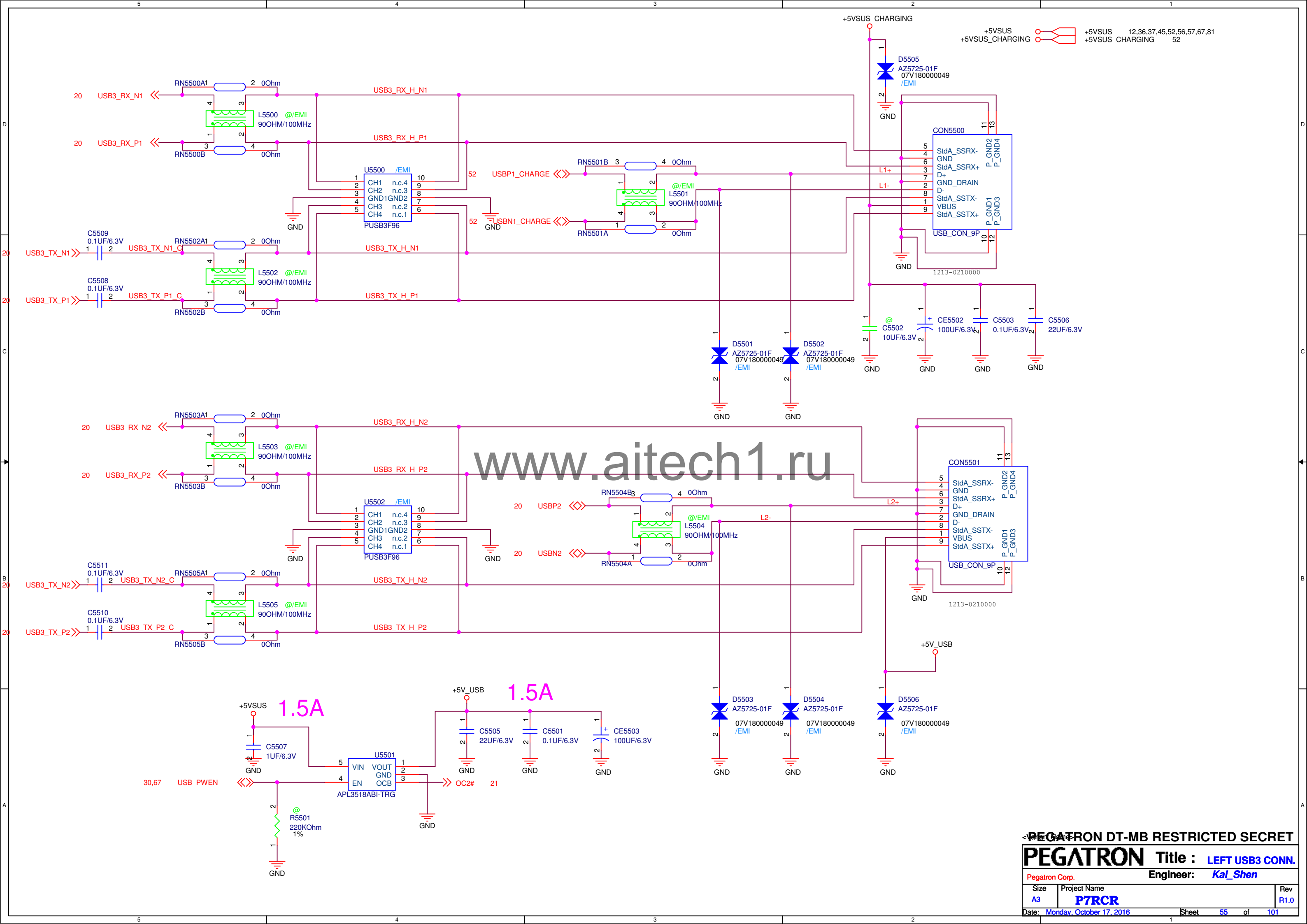
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : USB CHARGE IC	
Pegatron Corp.		Engineer: Kai_Shen	
Size A4	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 52	of 101

+5VA		+5VA	56,81
+3VSUS		+3VSUS	7,11,12,21,22,23,24,26,28,31,33,36,44,52,57,62,67,81,88,92
+3VS		+3VS	7,11,12,13,14,15,16,21,22,23,24,26,30,31,36,45,46,50,51,56,58,61,62,67,70,91,92

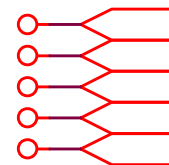


[illegible]

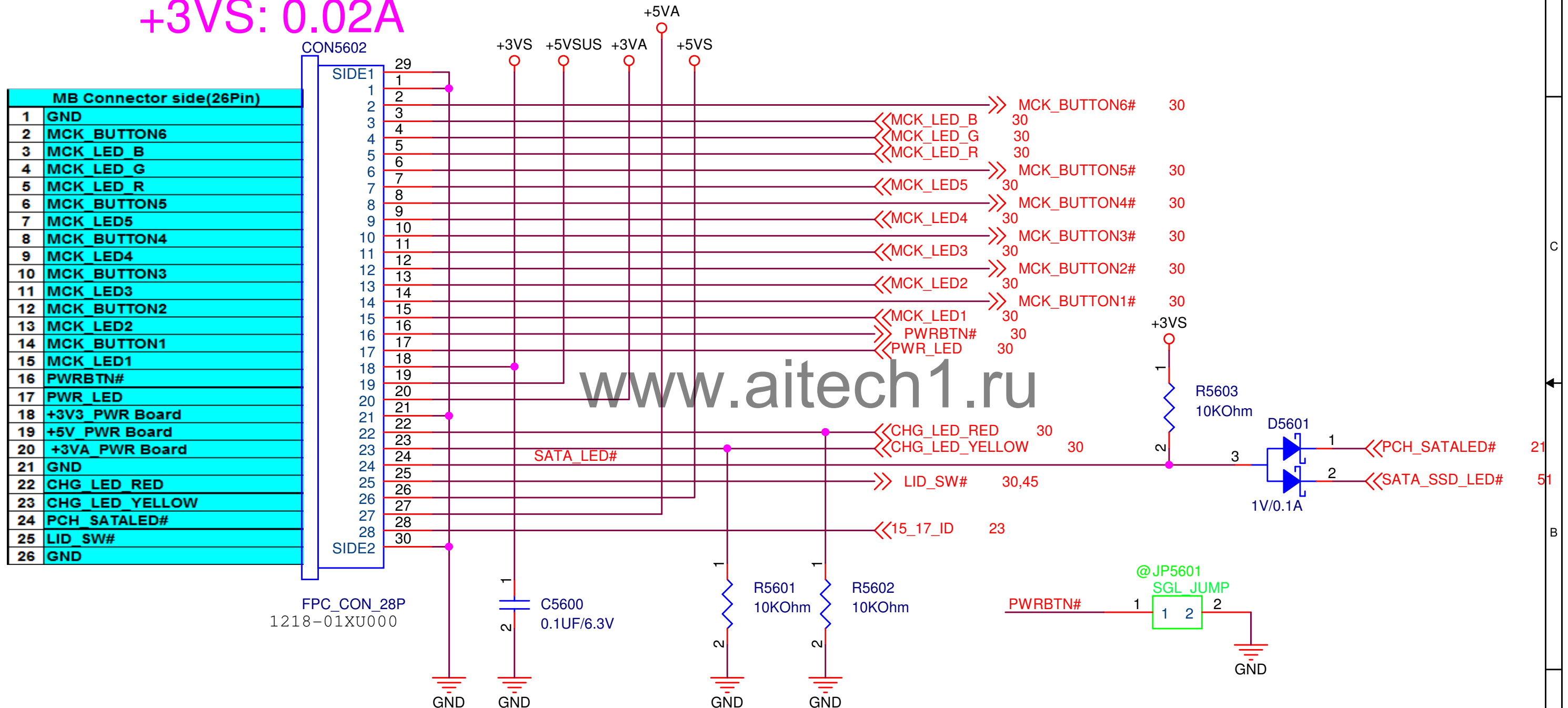


+5VA: 0.48A
+5VSUS: 0.225A
+5VS: 0.3A
+3VS: 0.02A

+3VS
+3VA
+5VA
+5VSUS
+5VS



+3VS 7,11,12,13,14,15,16,21,22,23,24,26,30,31,36,45,46,50,51,53,58,61,62,67,70,91,92
+3VA 26,30,44,45,57,60,81,88,93
+5VA 53,81
+5VSUS 12,36,37,45,52,55,57,67,81
+5VS 13,15,31,36,37,45,48,50,80,87,89,91,97

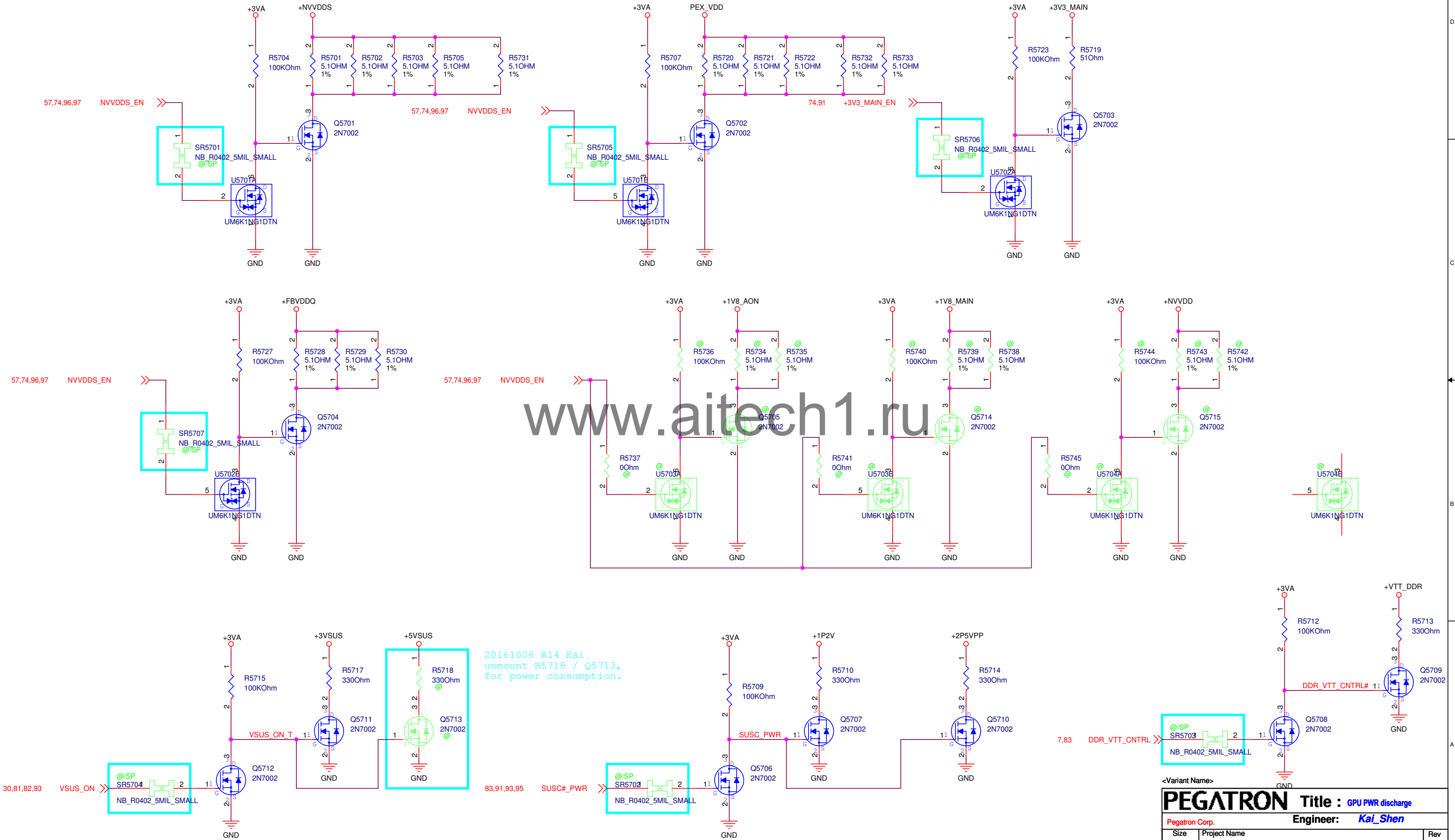


<Variant Name>

PEGATRON			Title : PWR BOARD CON		
Pegatron Corp.			Engineer: Kai_Shen		
Size A	Project Name P7RCR				Rev R1.0
Date: Monday, October 17, 2016			Sheet 56 of 101		

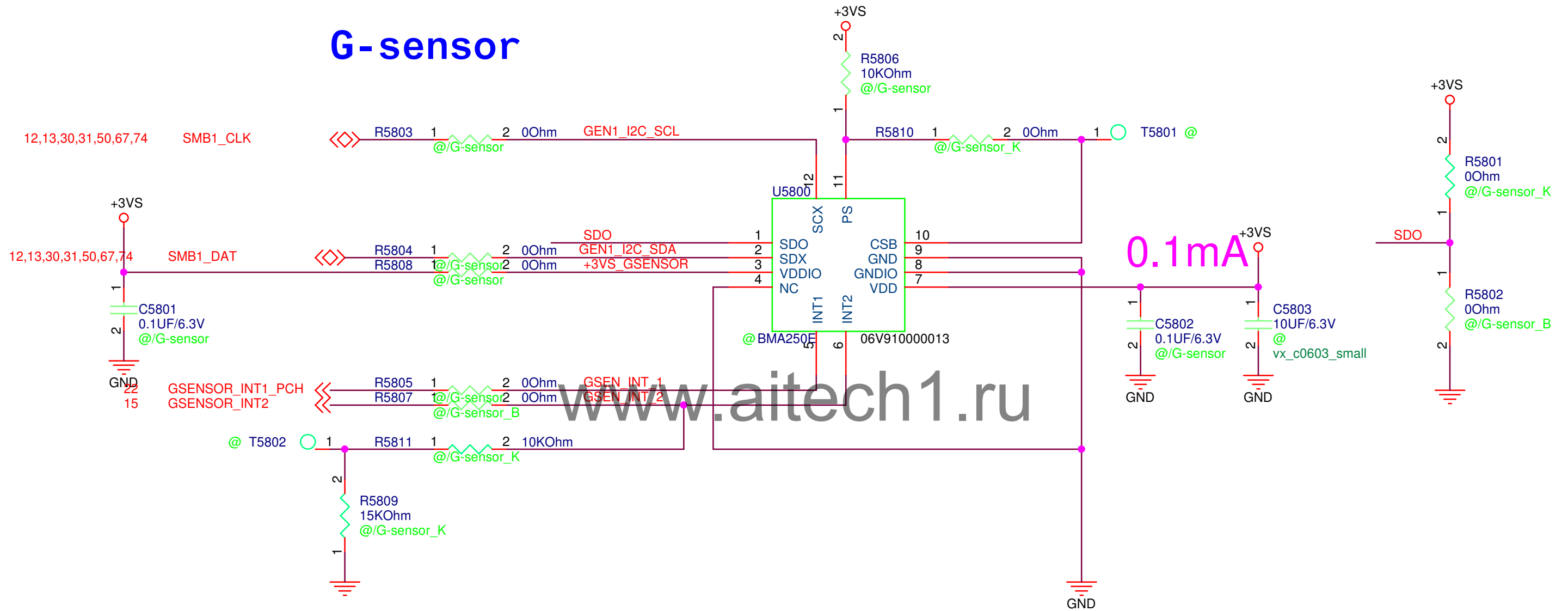
NV GPU POWER DISCHARGE

+3VA	26,30,44,45,56,60,81,88,93
+3VSUS	7,11,12,21,22,23,24,26,28,31,33,36,44,52,53,62,67,81,88,92
+5VSUS	12,36,37,45,52,55,56,67,81
+1P2V	7,10,13,16,17,24,83
+2P5VPP	16,17,18,95
+VTT_DDR	16,17,18,83
+NVVDDS	75,97
PEX_VDD	70,72,96
+FBVDDQ	71,75,76,77,78,79,89



20161006 R14 Kai
unmount R5718 / Q5713,
for power consumption.

G-sensor



<Variant Name>

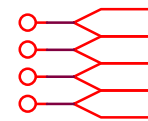
PEGATRON			Title :	G-sensor
Pegatron Corp.			Engineer:	Kai_Shen
Size A4	Project Name P7RCR			Rev R1.0
Date: Monday, October 17, 2016		Sheet	58	of 101

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 59 of 101	

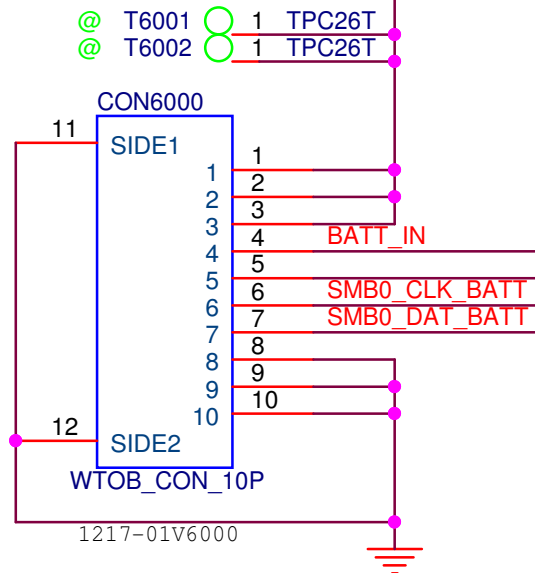
BATTERY CONNECTOR

+3VA
+BAT_CON
+A/D_DOCK_IN
+VCC_RTC



+3VA 26,30,44,45,56,57,81,88,93
+BAT_CON 88
+A/D_DOCK_IN 88
+VCC_RTC 24,26,28

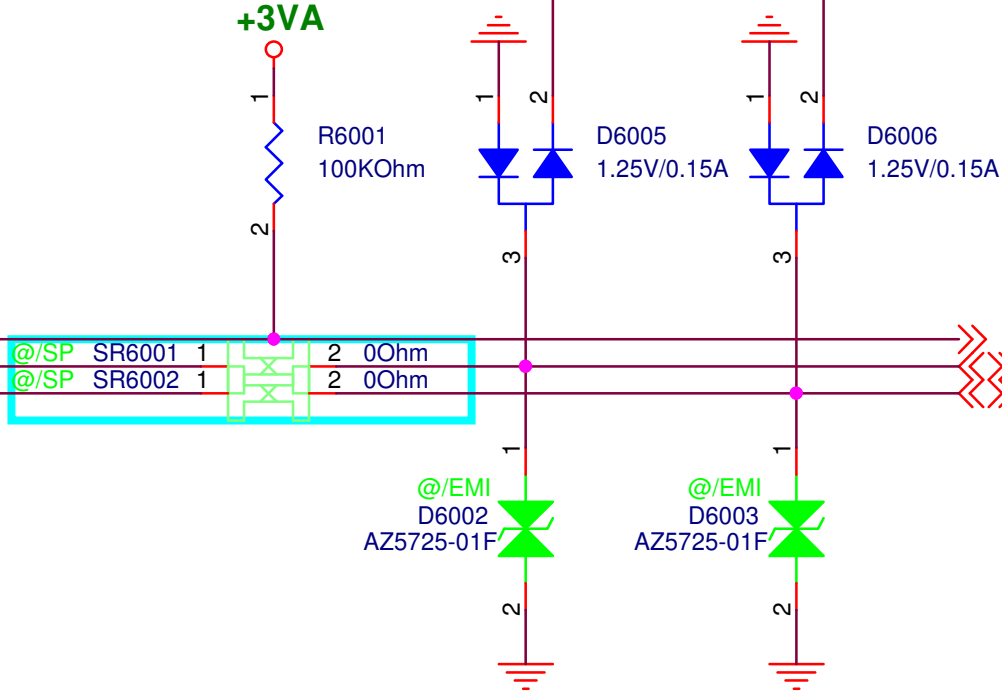
+BAT_CON



+3VA

+3VA

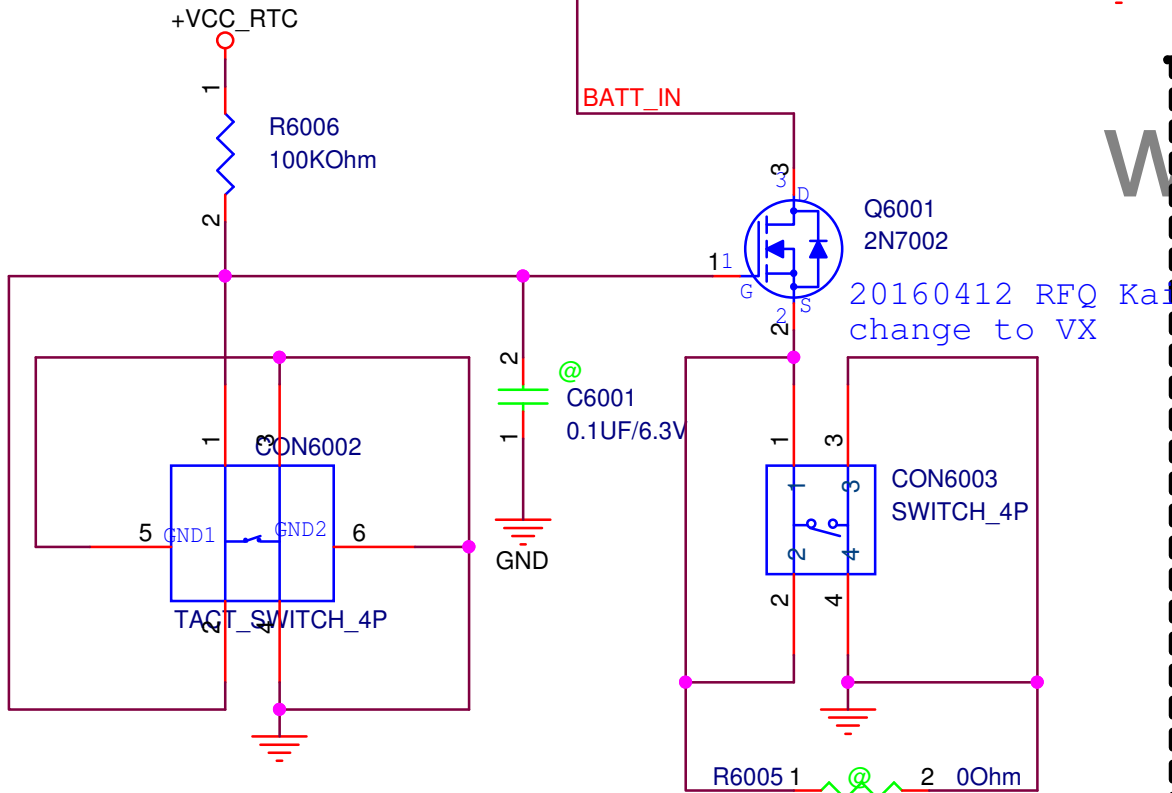
+3VA



TS1# 90
SMB0_CLK 30,88
SMB0_DAT 30,88

+VCC_RTC

BATT_IN

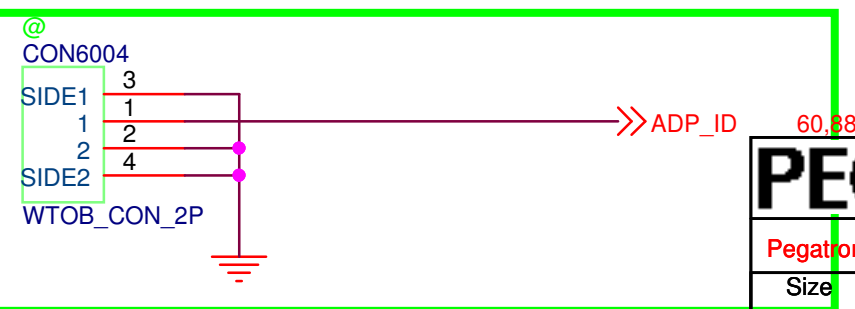
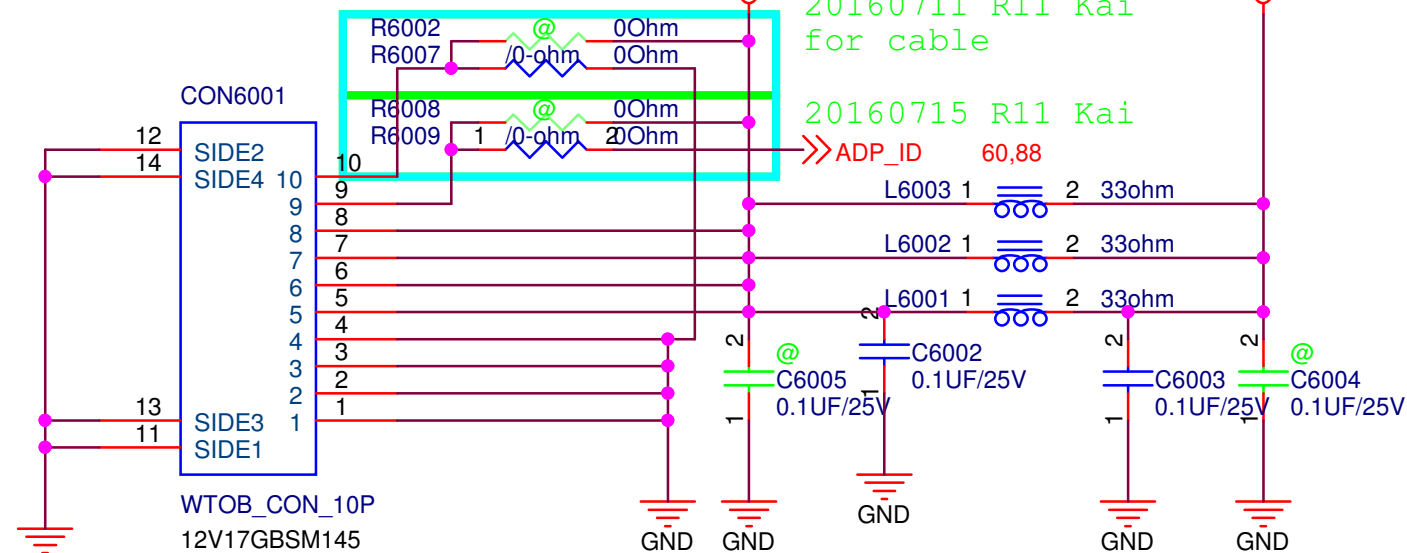


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AC IN CONNECTOR

+A/D_DOCK_IN_CON

+A/D_DOCK_IN



20160711 R1.1 Kai
for cable
20160715 R1.1 Kai
ADP_ID 60,88
20160718 R1.1 Kai, add CON6004
20160719 R1.1 Kai, unmount CON6004

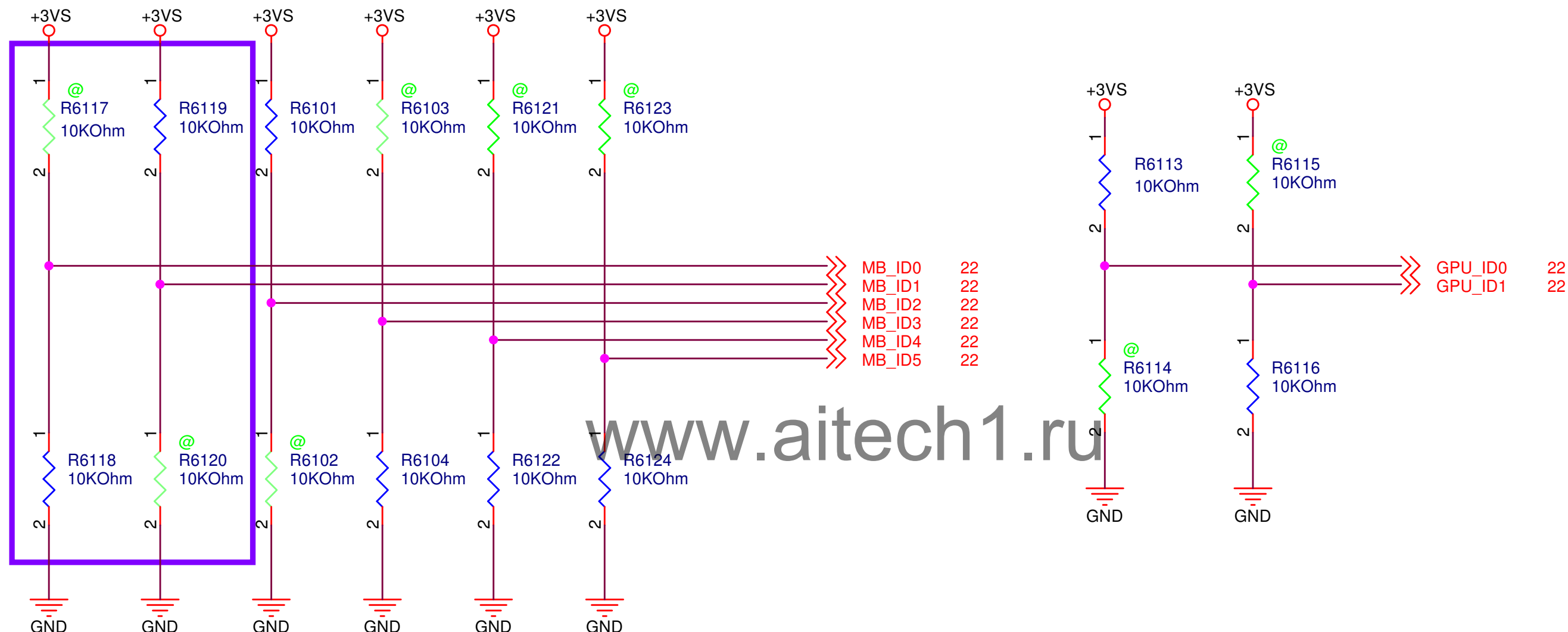
PEGATRON Title : BATT CON/AC IN

Pegatron Corp. Engineer: Kai_Shen

Size A4 Project Name P7RCR Rev R1.0

Date: Monday, October 17, 2016 Sheet 60 of 101

20161013 R20 Kai
Change for R20 PCB ID setting



MB_ID2 (GPP_G6)	MB_ID1 (GPP_G5)	MB_ID0 (GPP_G4)	
0	0	0	R1.0
0	0	1	R1.1
0	1	0	R1.2
1	0	0	R1.3
1	0	1	R1.4
1	1	0	R2.0
1	1	1	R2.1
0	0	0	R2.2

	QLM4, 2.9G 0101-03FG0PB	QLM5, 2.8G 0101-03EY0PB
GPP_G10 (ID0)	1	0
GPP_G11 (ID1)	0	0

PEGATRON
Title : BOARD ID

Pegatron Corp.
Engineer: Kai_Shen

Size
A

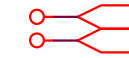
Project Name
P7RCR

Rev
R1.0

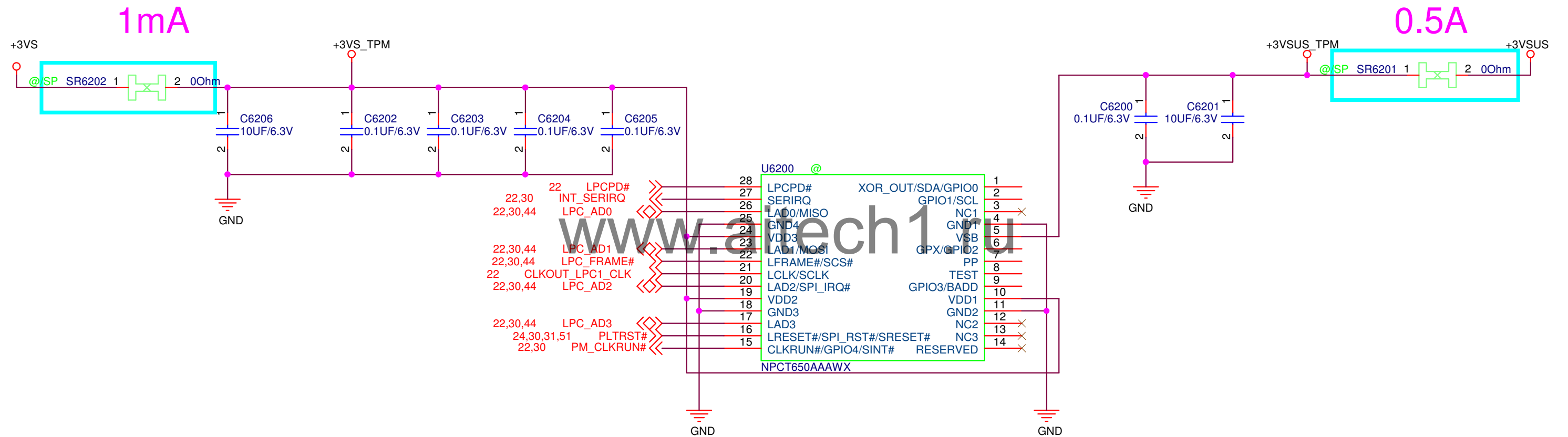
Date: Monday, October 17, 2016
Sheet 61 of 101

NPCT650

+3VS
+3VSUS



+3VS	7,11,12,13,14,15,16,21,22,23,24,26,30,31,36,45,46,50,51,53
+3VSUS	7,11,12,21,22,23,24,26,28,31,33,36,44,52,53,57,67,81,88



<Variant Name>

PEGATRON			Title : <i>TPM</i>		
Pegatron Corp.			Engineer: <i>Kai_Shen</i>		
Size <i>Custom</i>	Project Name <i>P7RCR</i>				Rev <i>R1.0</i>
Date: <i>Monday, October 17, 2016</i>		Sheet <i>62</i> of <i>101</i>			

[illegible]

5 4 3 2 1

D

C

B

A

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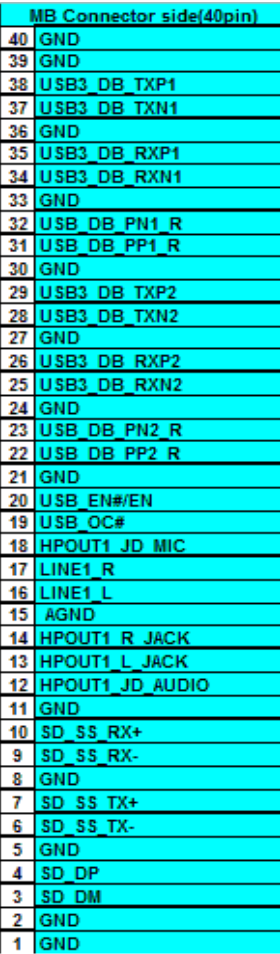
PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 64 of 101	

5 4 3 2 1

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 65 of 101	

Size A		Project Name P7RCR		Rev R1.0	
Date: Monday, October 17, 2016		Sheet 66 of 101			



MB Connector side(5pin)	
1	+3VS_DB
2	+3VS_DB
3	+5V_POWER
4	+5V_POWER
5	+5V_POWER

REGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : IO BOARD COM

Pegatron Corp. **Engineer:** *Kai_Shen*

Size Custom	Project Name P7RCR	Revised By R
Date: Monday, October 17, 2016		Sheet 67 of 101

PEGATRON

Title : DDR3 TERMINATION A&B

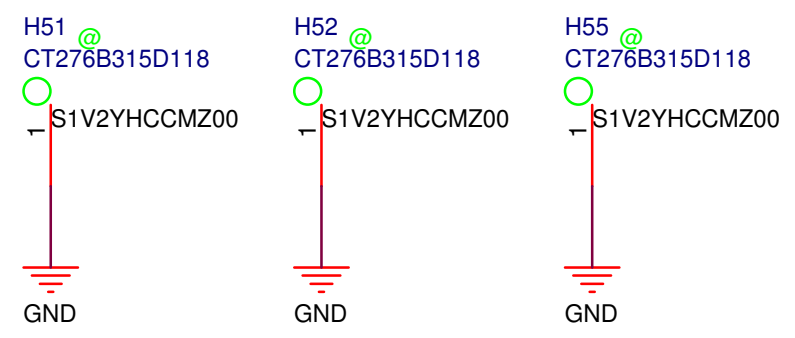
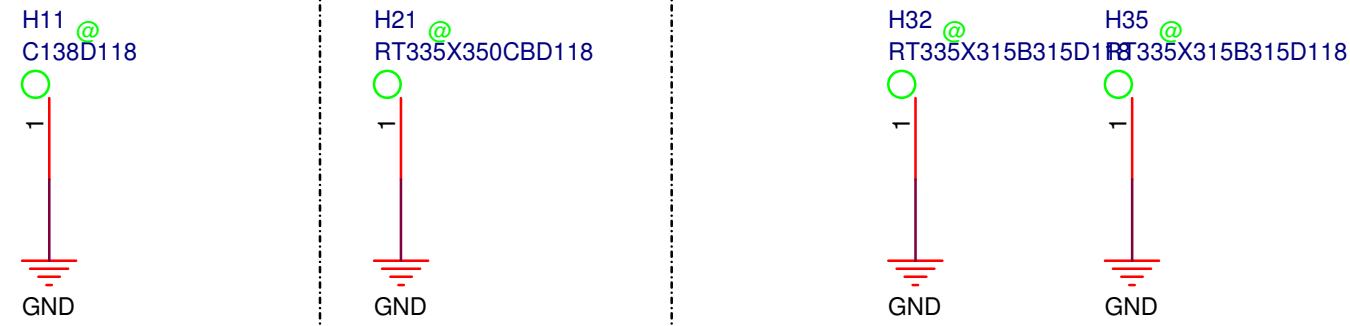
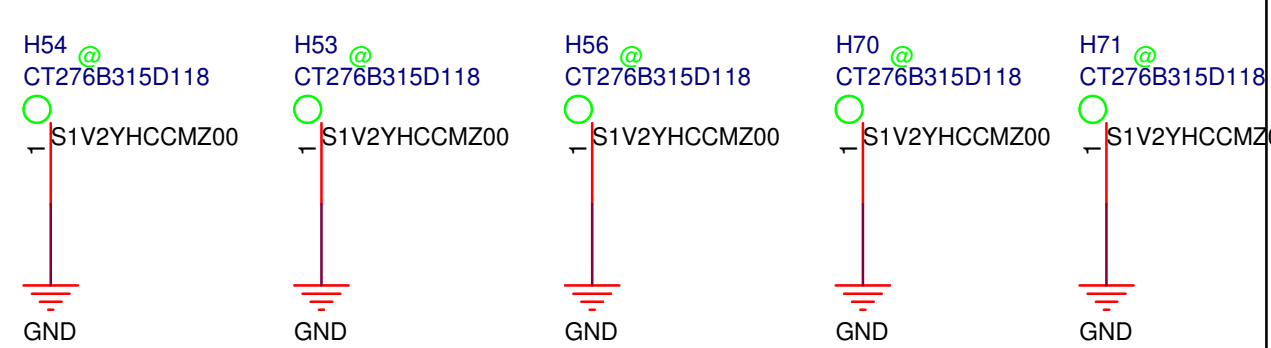
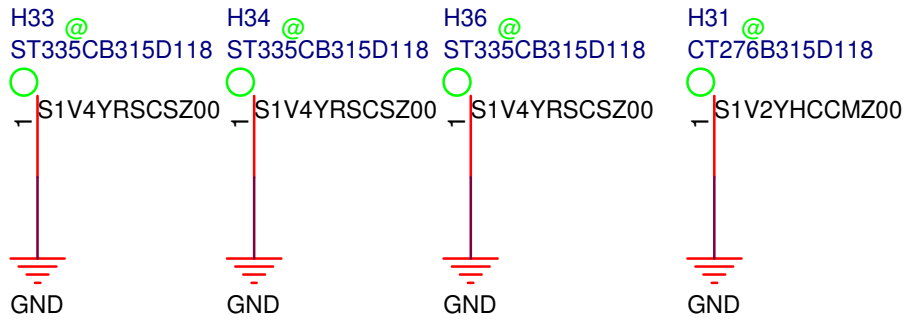
Pegatron Corp.

Engineer: Kai_Shen

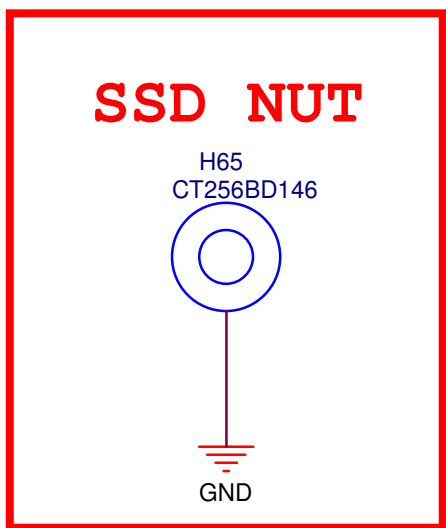
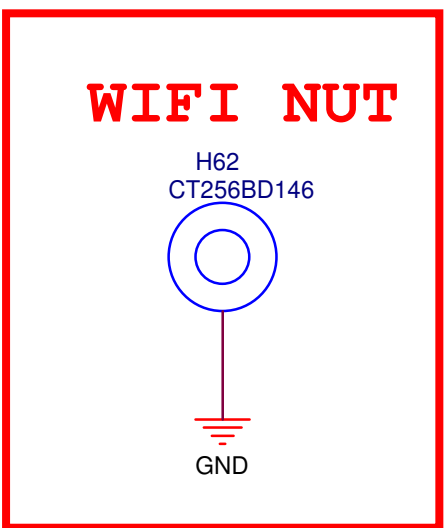
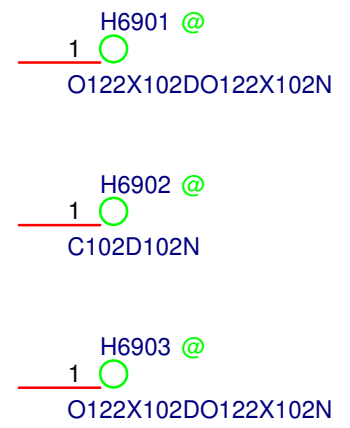
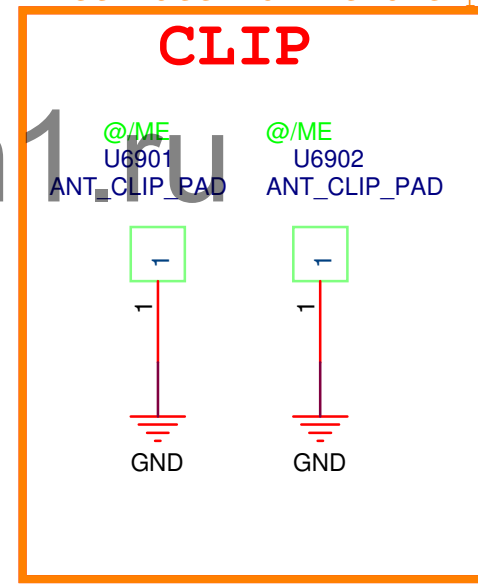
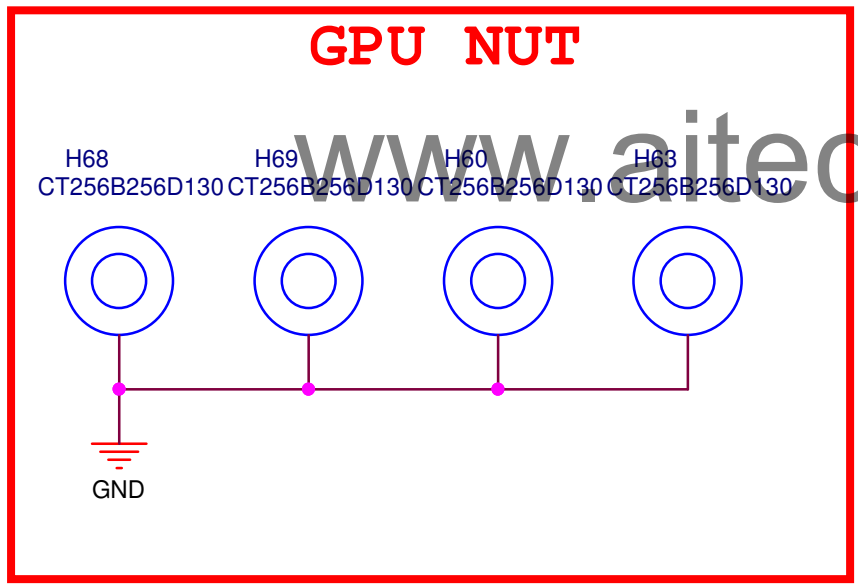
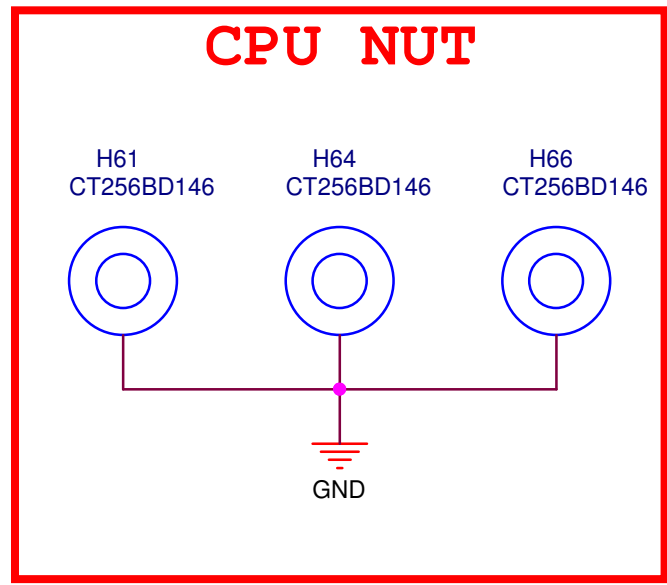
Size	Project Name	Rev
A	P7RCR	R1.0

Date: Monday, October 17, 2016

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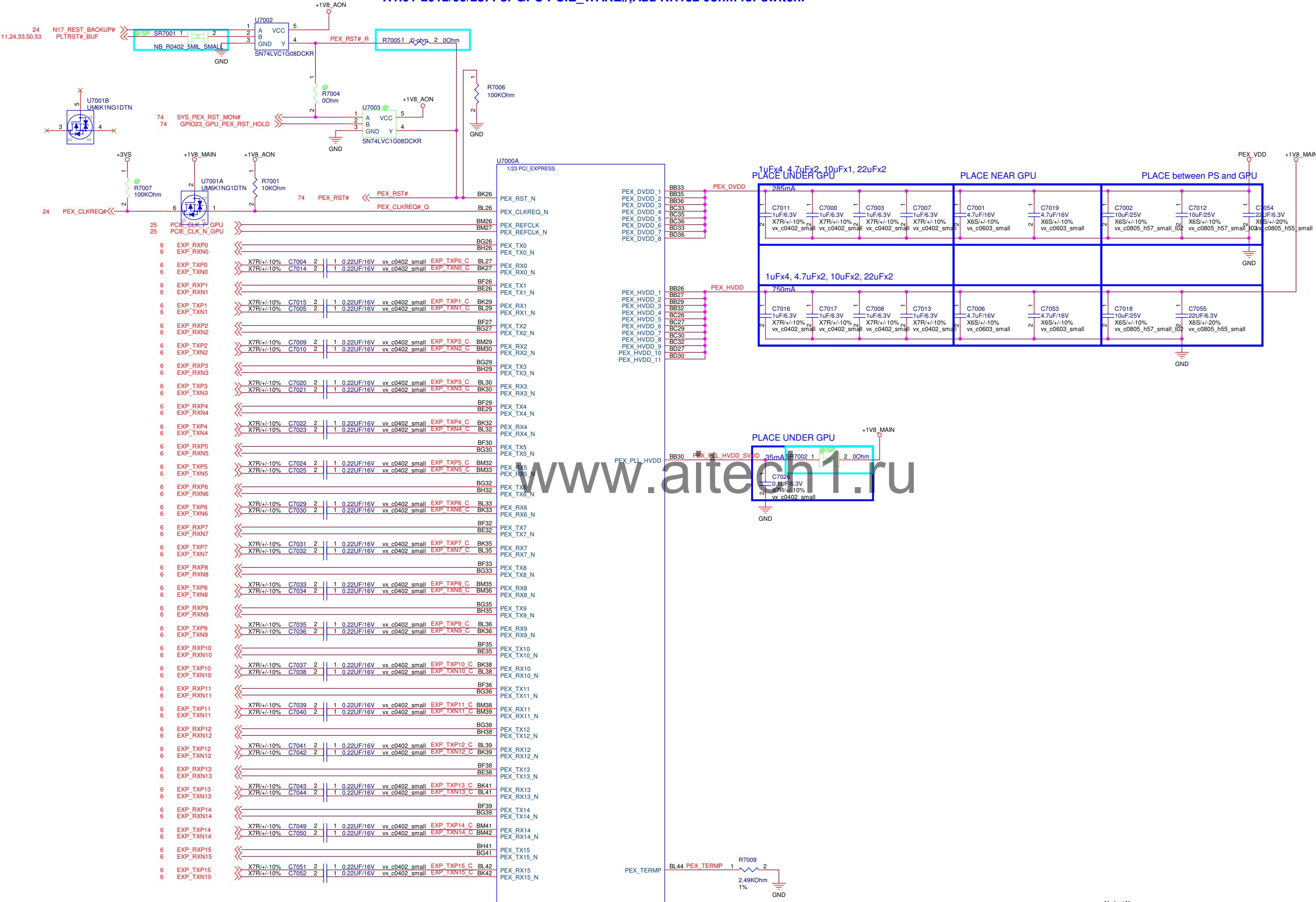
20160517 WS Kai
unomunt for ME request
retimate for remove parts after B-build



PCI-Express Gen3 x 16 Interface

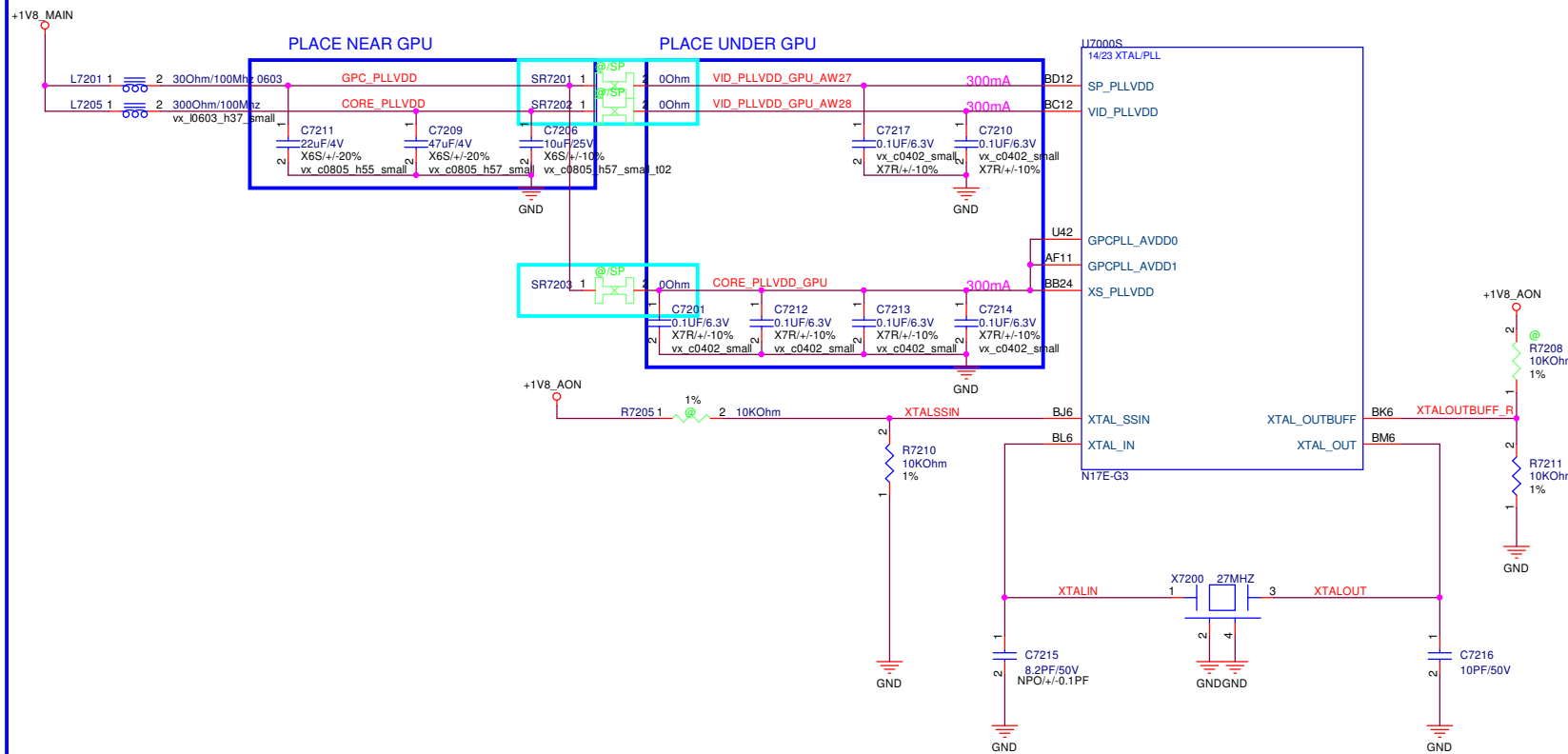
R1.01-2012/09/26:add C9972 220pf "NI" for GPU "PCIE_RST#"
R1.01-2012/09/28: For GPU PCIE_WAKE#,Add NR132 0ohm for switch.

+1V8_AON
+1V8_MAIN
PEX_VDD
+3VS

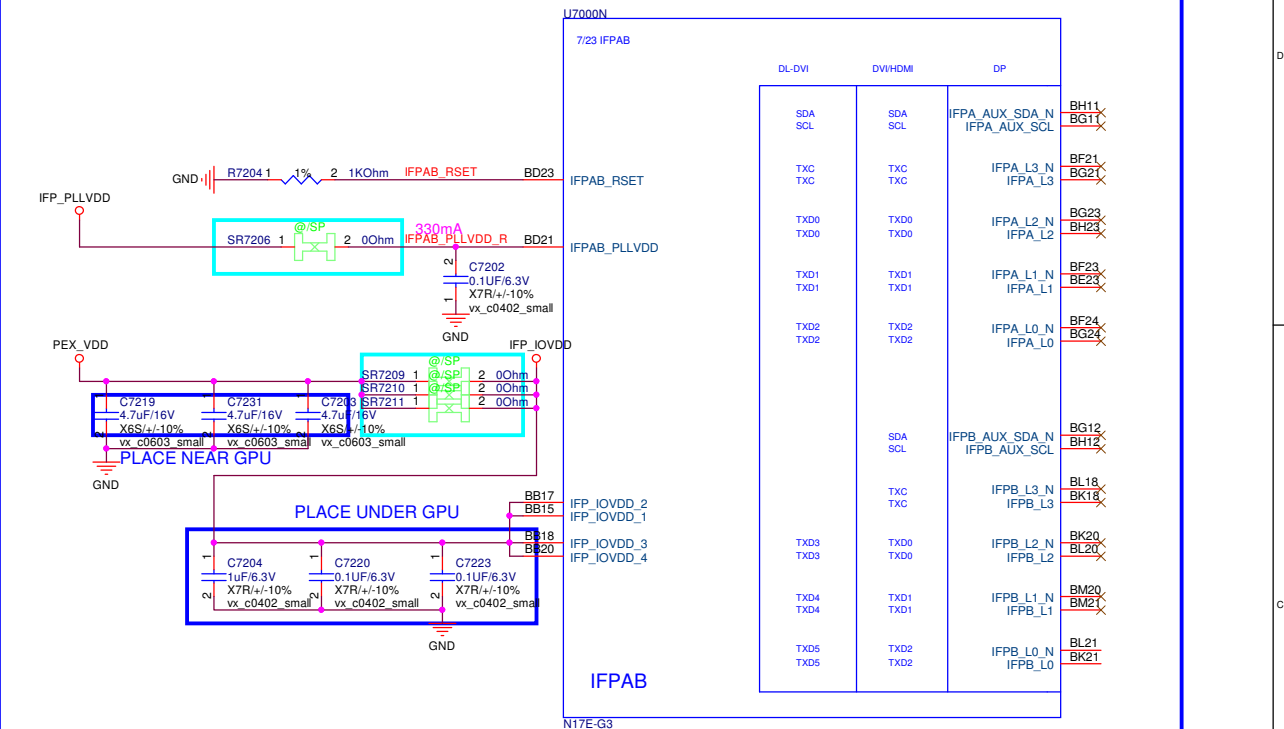


20160419 RFQ Kai
Follor CRB
Add R7202, R7203, R7206, R7207, R7209, R7215, R7222, R7223, R7224

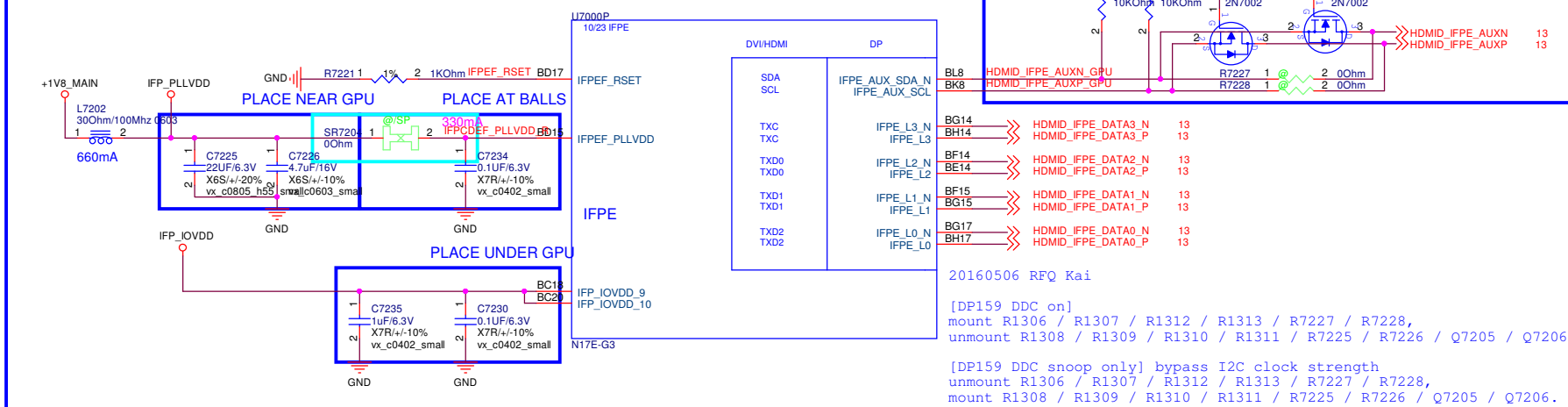
GPU Xtal



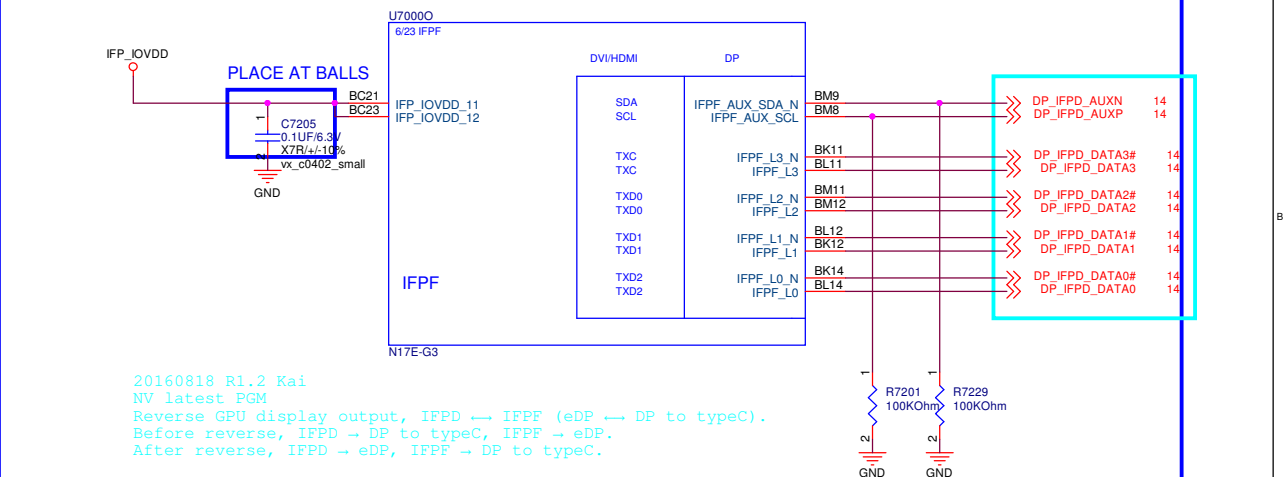
Display export - N/A



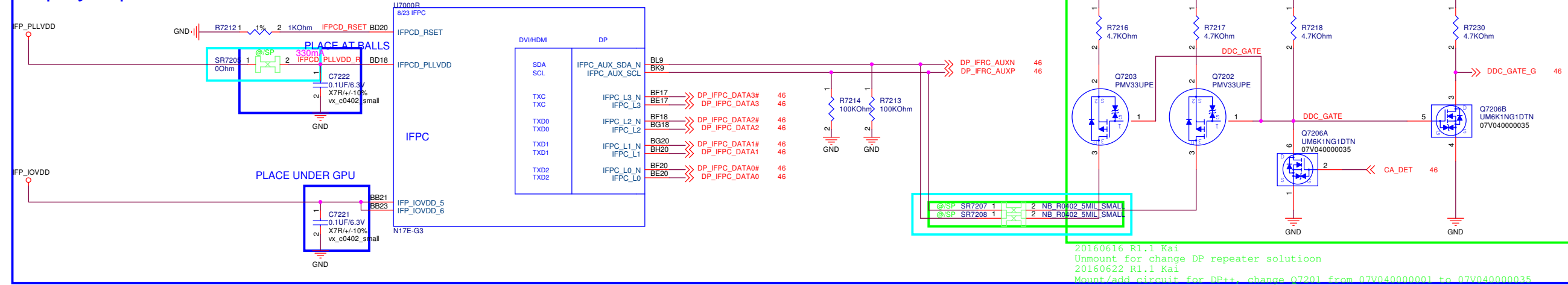
Display export - HDMI connector



Display export - DP to Type C connector



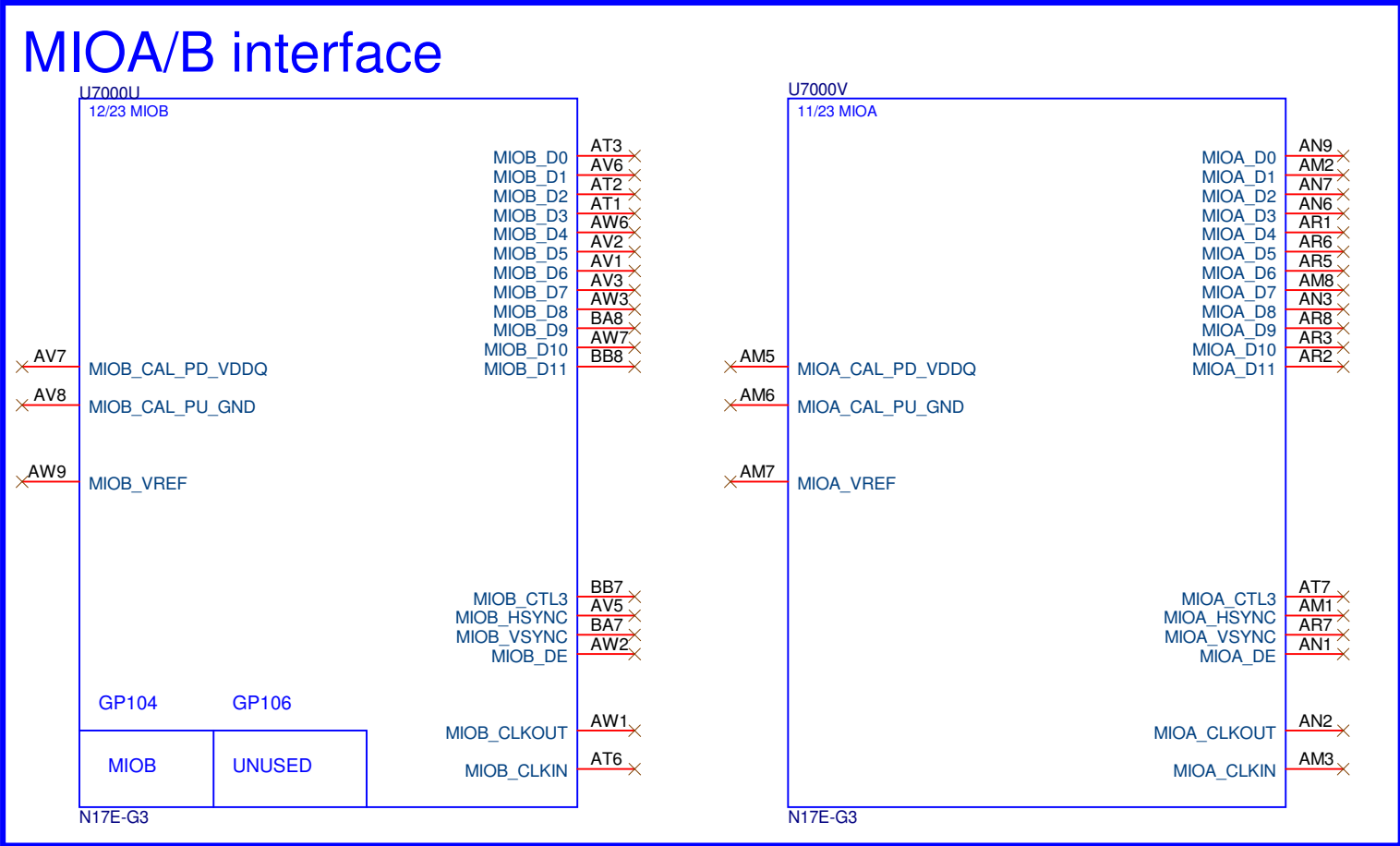
Display export - DP connector



<Variant Name>

PEGATRON Title : NVIDIA/DACA/XTAL

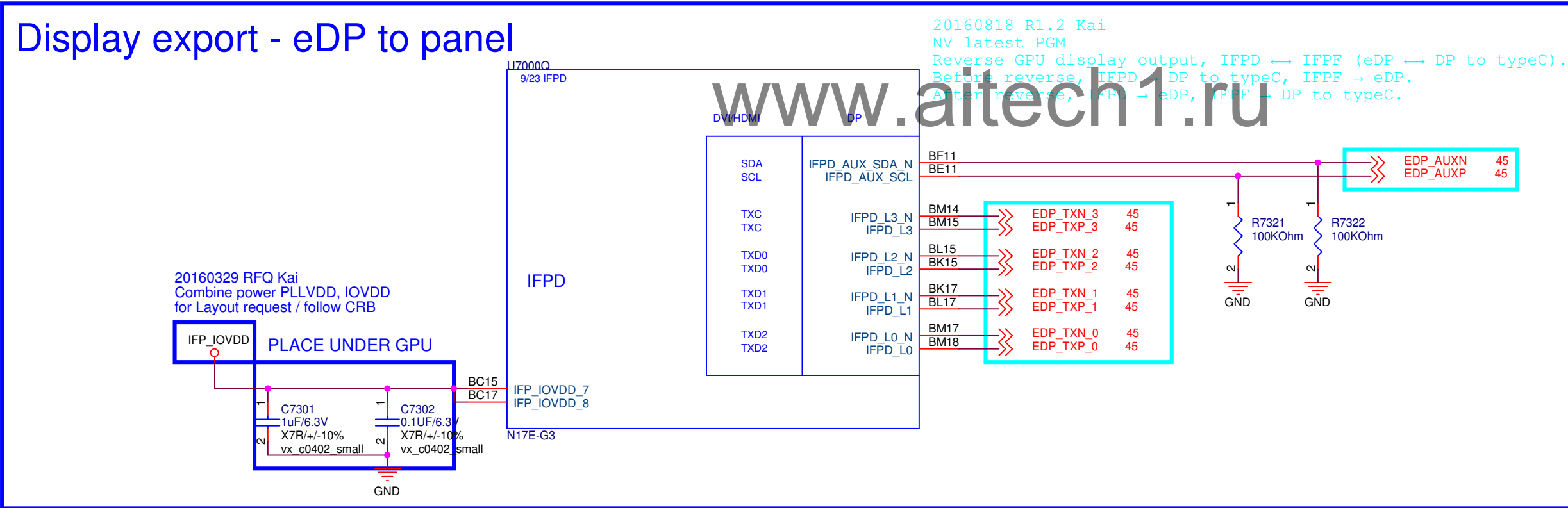
Pegatron Corp.		Engineer: Kai_Shen	
Size A2	Project Name P7RCR	Rev R1.0	
Date: Monday, October 17, 2016		Sheet 72 of 101	



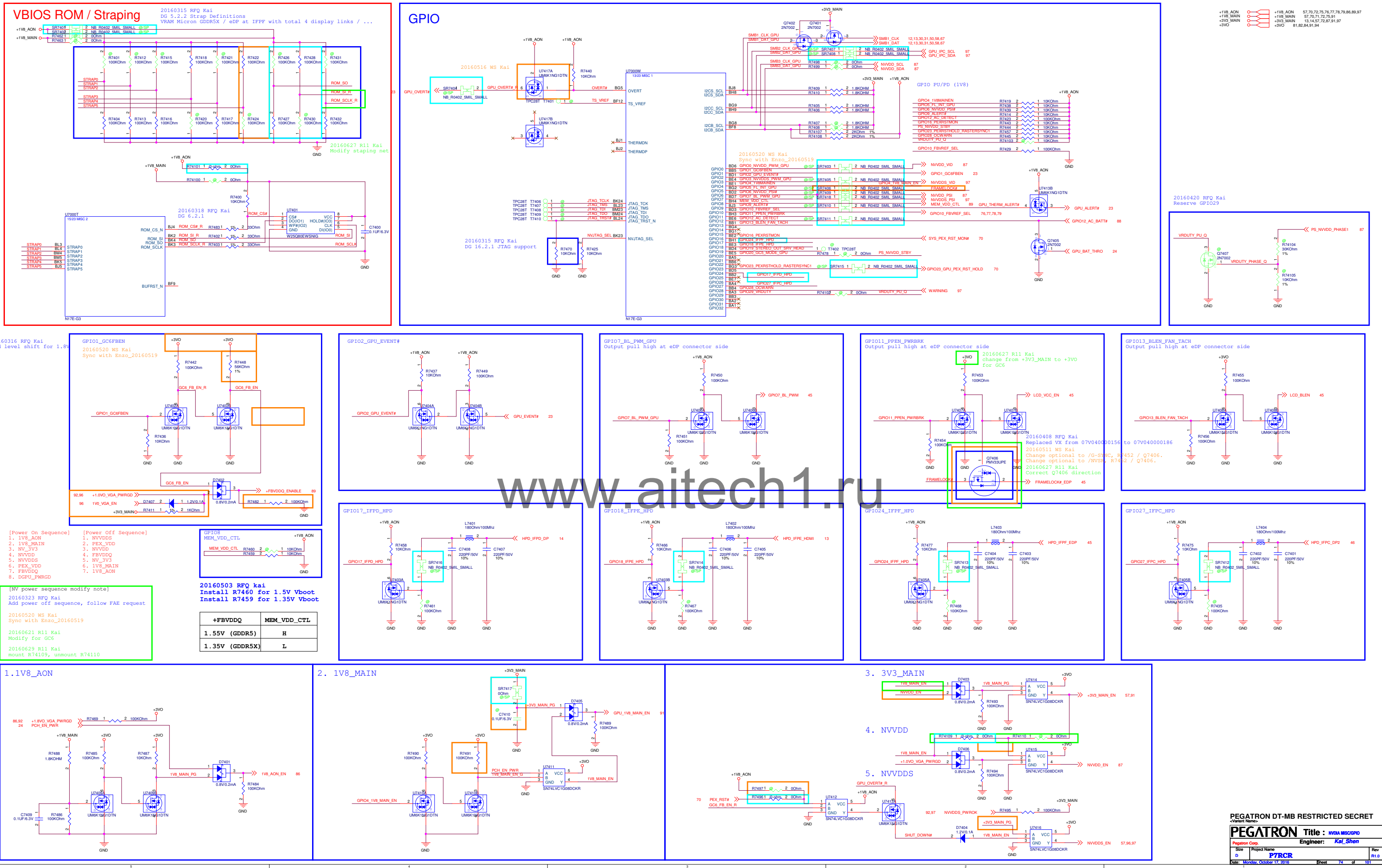
PEX_VDD
IFP_IOVDD

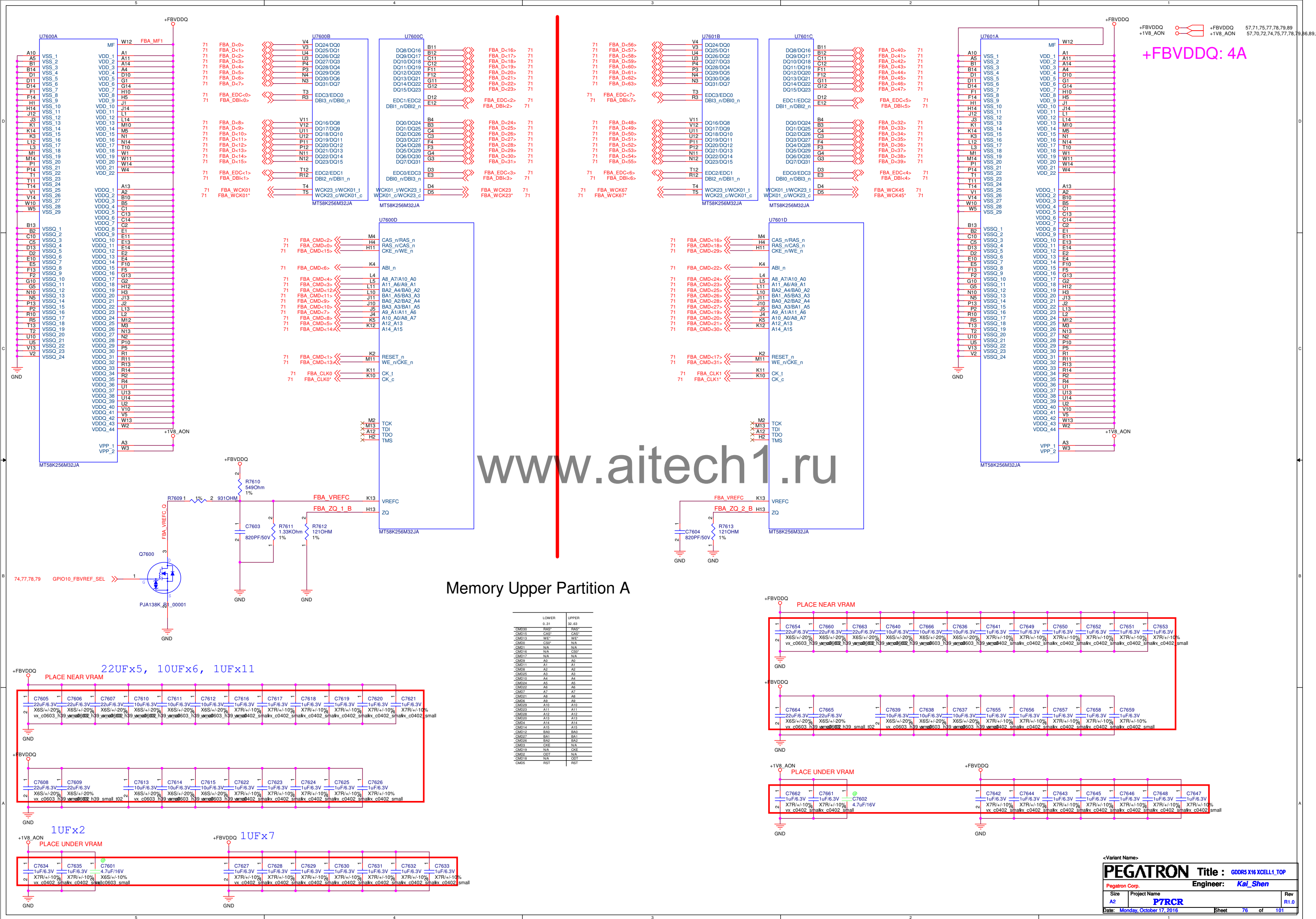
PEX_VDD
IFP_IOVDD

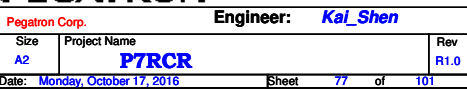
57,70,72,96
72

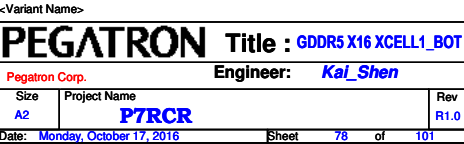


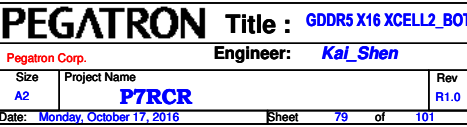
20160818 R1.2 Kai
NV latest PGM
Reverse GPU display output, IFPD ↔ IFPF (eDP ↔ DP to typeC).
Before reverse, IFPD → DP to typeC, IFPF → eDP.
After reverse, IFPD → eDP, IFPF → DP to typeC.





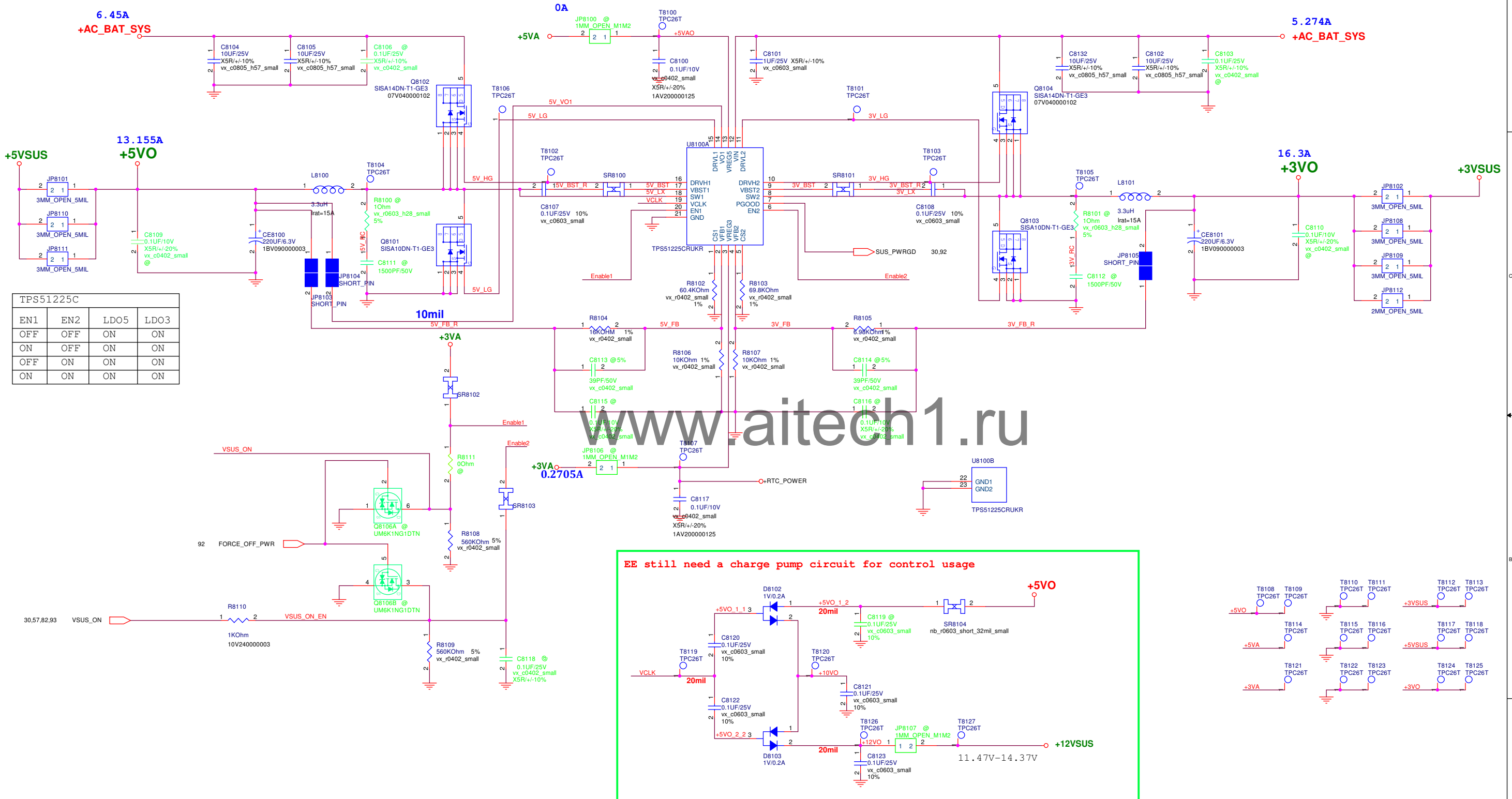




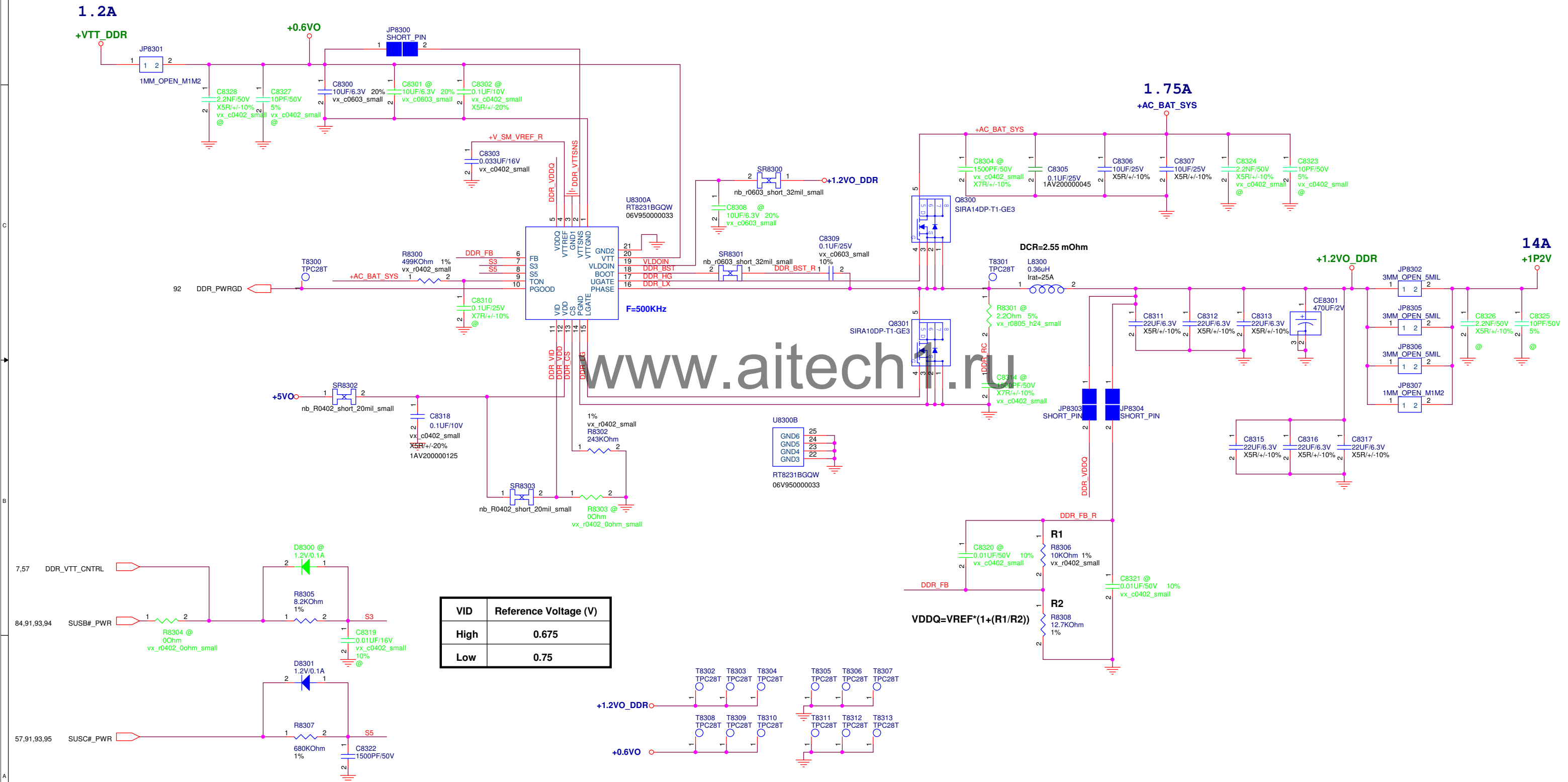




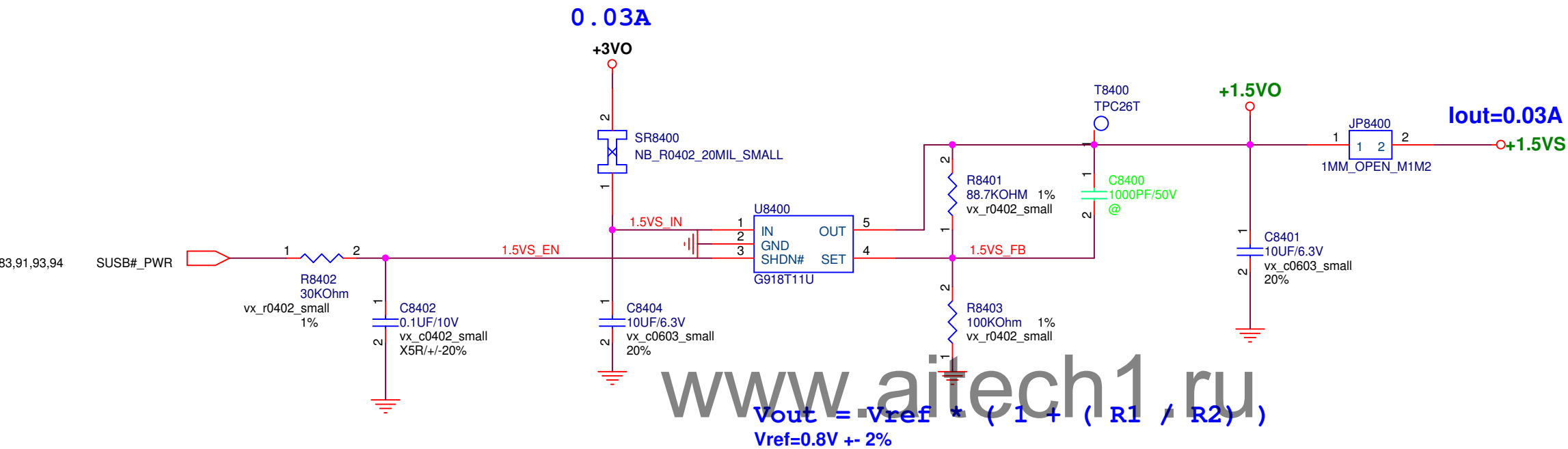
+5VO & +3VO POWER SUPPLY



DDR & VTT POWER SUPPLY



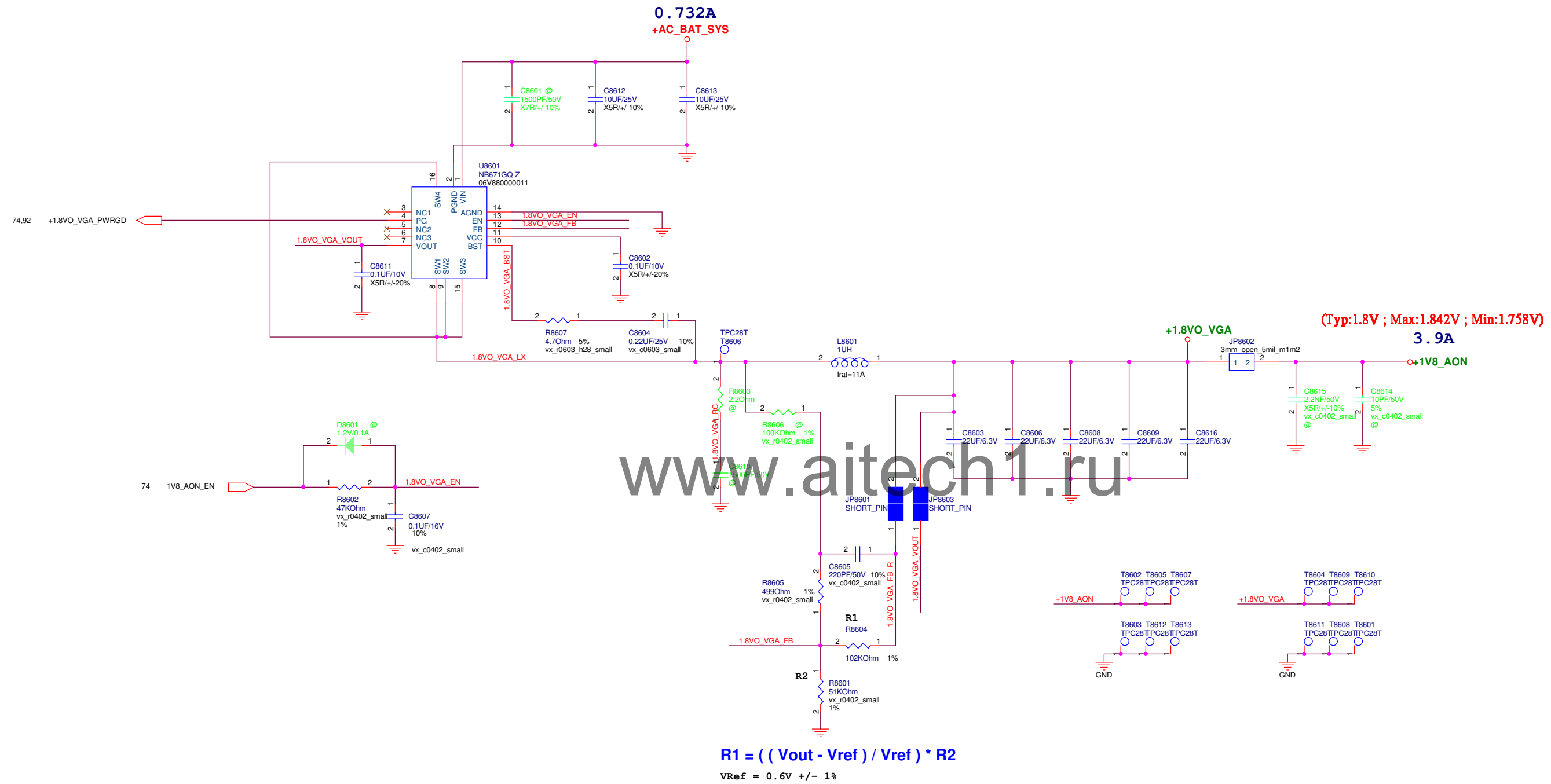
1.5V POWER SUPPLY



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PEGATRON		Title : USB CHARGE IC	
Pegatron Corp.		Engineer: Shrek_Tseng	
Size Custom	Project Name IPPSL-CD		Rev A00
Date: Monday, October 17, 2016		Sheet 85 of 108	

1V8_VGA POWER SUPPLY



+NVVDD POWER SUPPLY

N17-G3		
R1	R8705	6.19K
R2	R8706	20.5K
R3	R8707	4.32K
R4	R8708	16.5K
R5	R8709	309
C	C8701	4700PF
	Vmin	0.3V
	Vmax	1.3V
	Vboot	0.8V
	VSTB	6.25mV

PWMVDD CIRCUIT

+NVVDD, VREF

+NVVDD, REFADJ

+NVVDD, REFIN

+3V3_MAIN+3V3_MAIN+5VS

+3V3_MAIN

+AC_BAT_SYS_NVVDD

12. 6A

+AC_BAT_SYS_NVVDD

EDPC=121A

+NVVDD

+NVVDD

+NVVDD

+NVVDD

+NVVDD

+AC_BAT_SYS_NVVDD

+AC_BAT_SYS_NVVDD

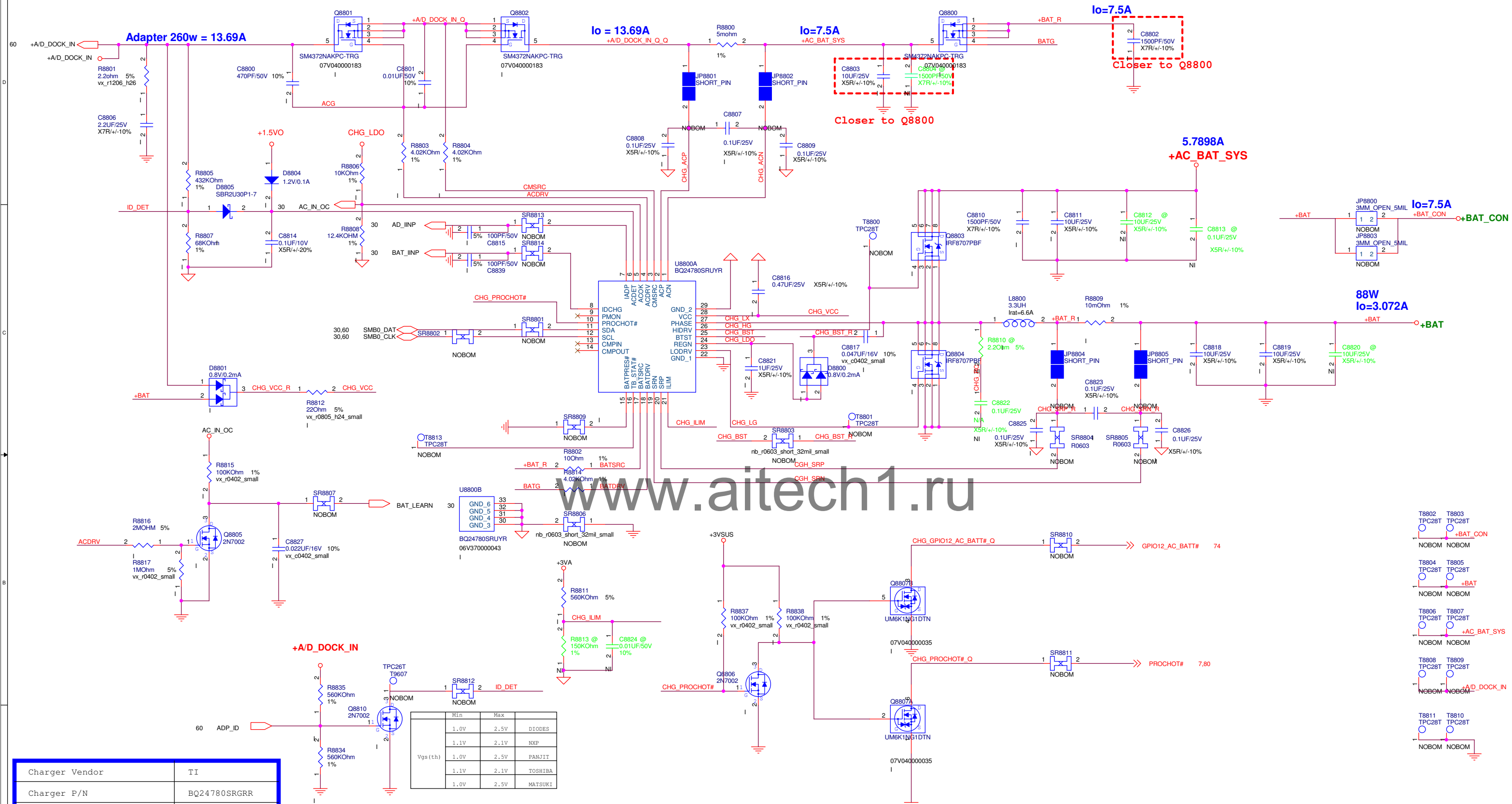
+AC_BAT_SYS_NVVDD

+AC_BAT_SYS_NVVDD

+AC_BAT_SYS_NVVDD

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BATTERY CHARGER



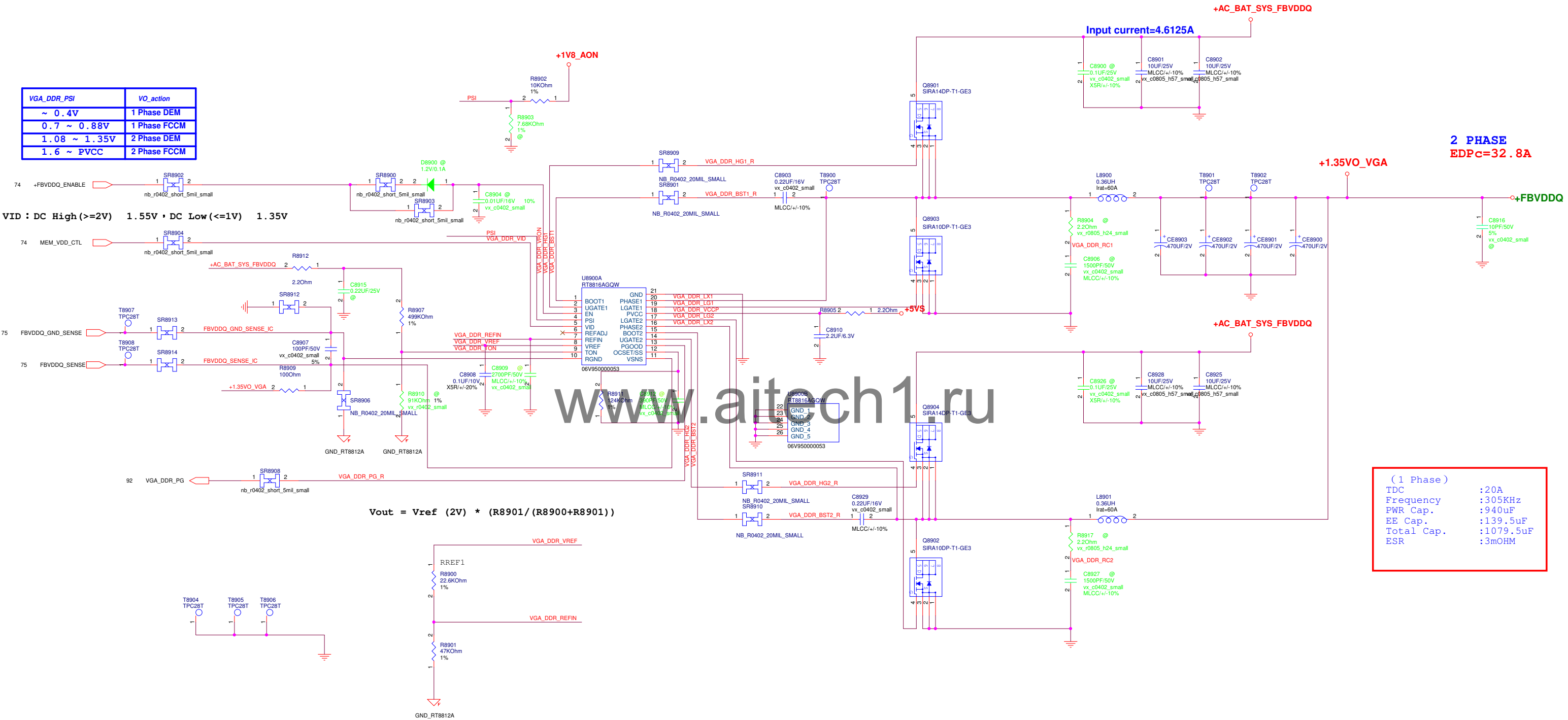
Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	260W
Active/Release Point (Hybrid Boost)	Active - 250.38W Release - 217.62W
Enable condition Disable condition	RSOC>40% RSOC<30%

	Min	Max	
Vgs(th)	1.0V	2.5V	DIODES
	1.1V	2.1V	NXP
	1.0V	2.5V	PANJIT
	1.1V	2.1V	TOSHIBA
	1.0V	2.5V	MATSUKI

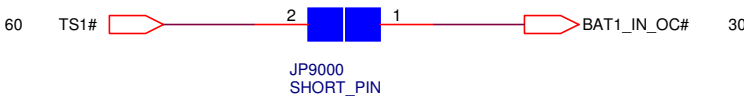
+FBVDDQ POWER SUPPLY

VGA_DDR_PSI	VO_action
~ 0.4V	1 Phase DEM
0.7 ~ 0.88V	1 Phase FCCM
1.08 ~ 1.35V	2 Phase DEM
1.6 ~ PVCC	2 Phase FCCM

VID : DC High (>=2V) 1.55V , DC Low (<=1V) 1.35V



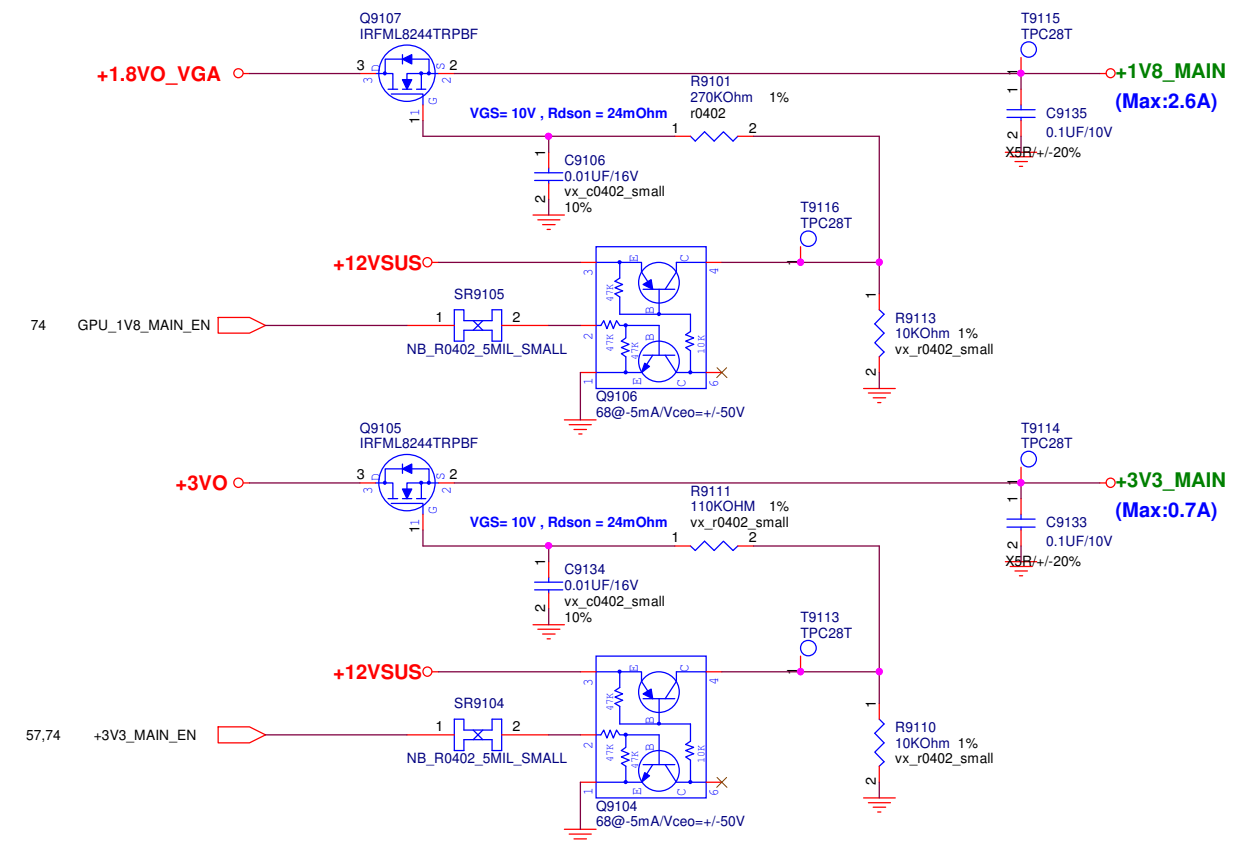
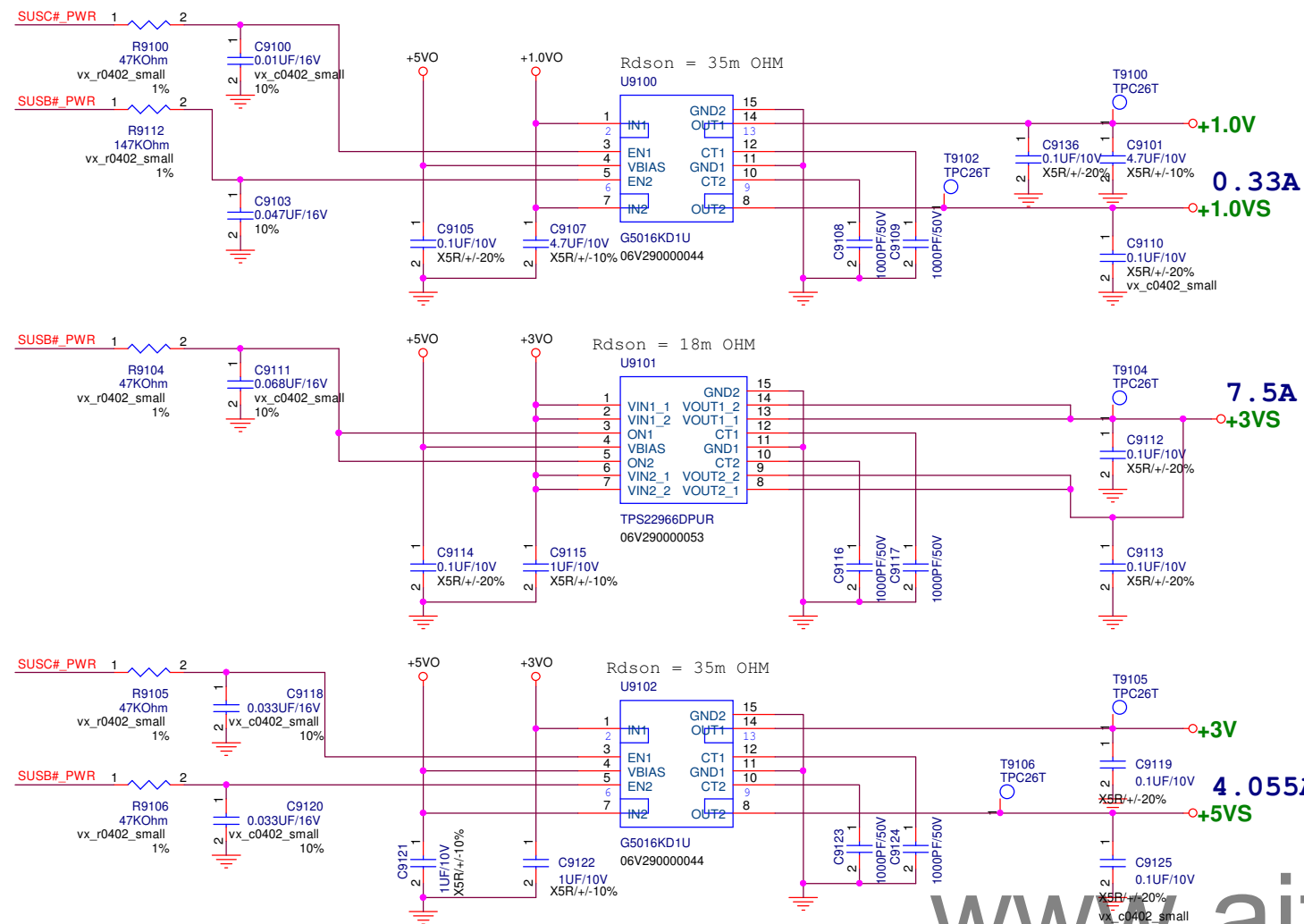
BATTERY IN DETECT



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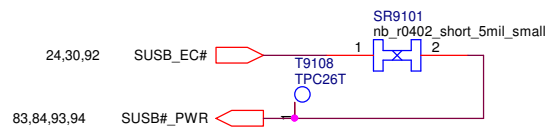
SUSB#_PWR POWER

SUSC#_PWR POWER

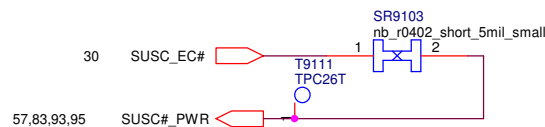


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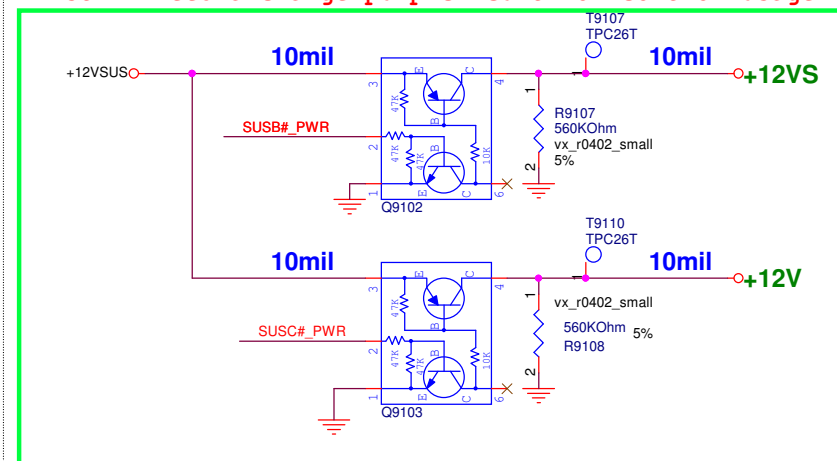
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control

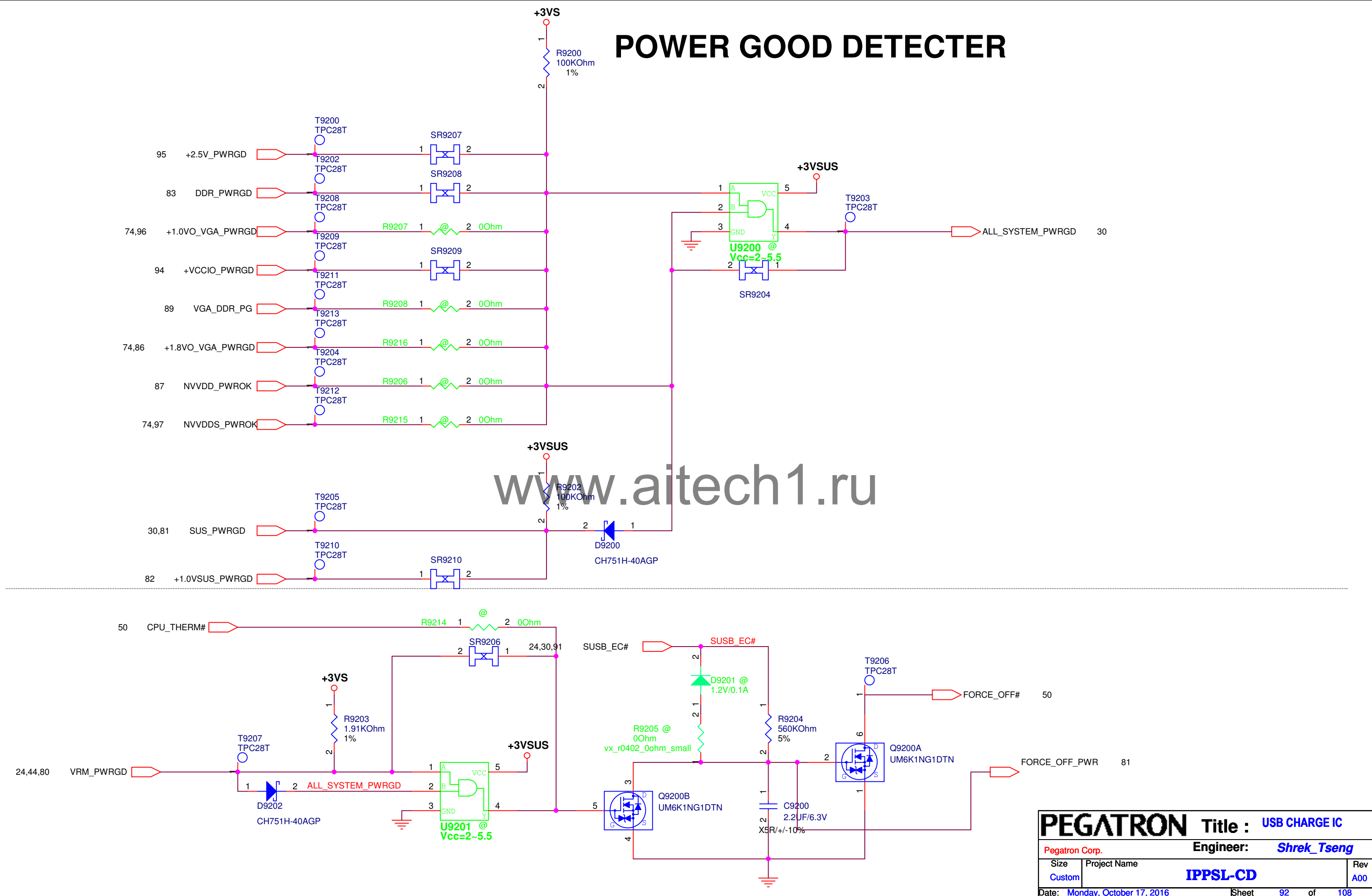


EE still need a charge pump circuit for control usage



PEGATRON Title : USB CHARGE IC		
Pegatron Corp.	Engineer:	Shrek Tseng
Size	Project Name	Rev
Custom	IPPSL-CD	A00
Date: Monday, October 17, 2016	Sheet	91 of 108

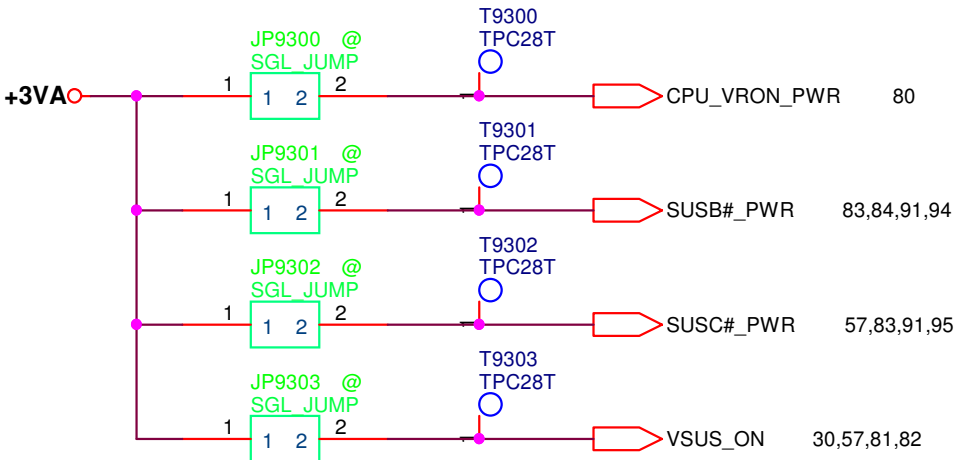
POWER GOOD DETECTOR



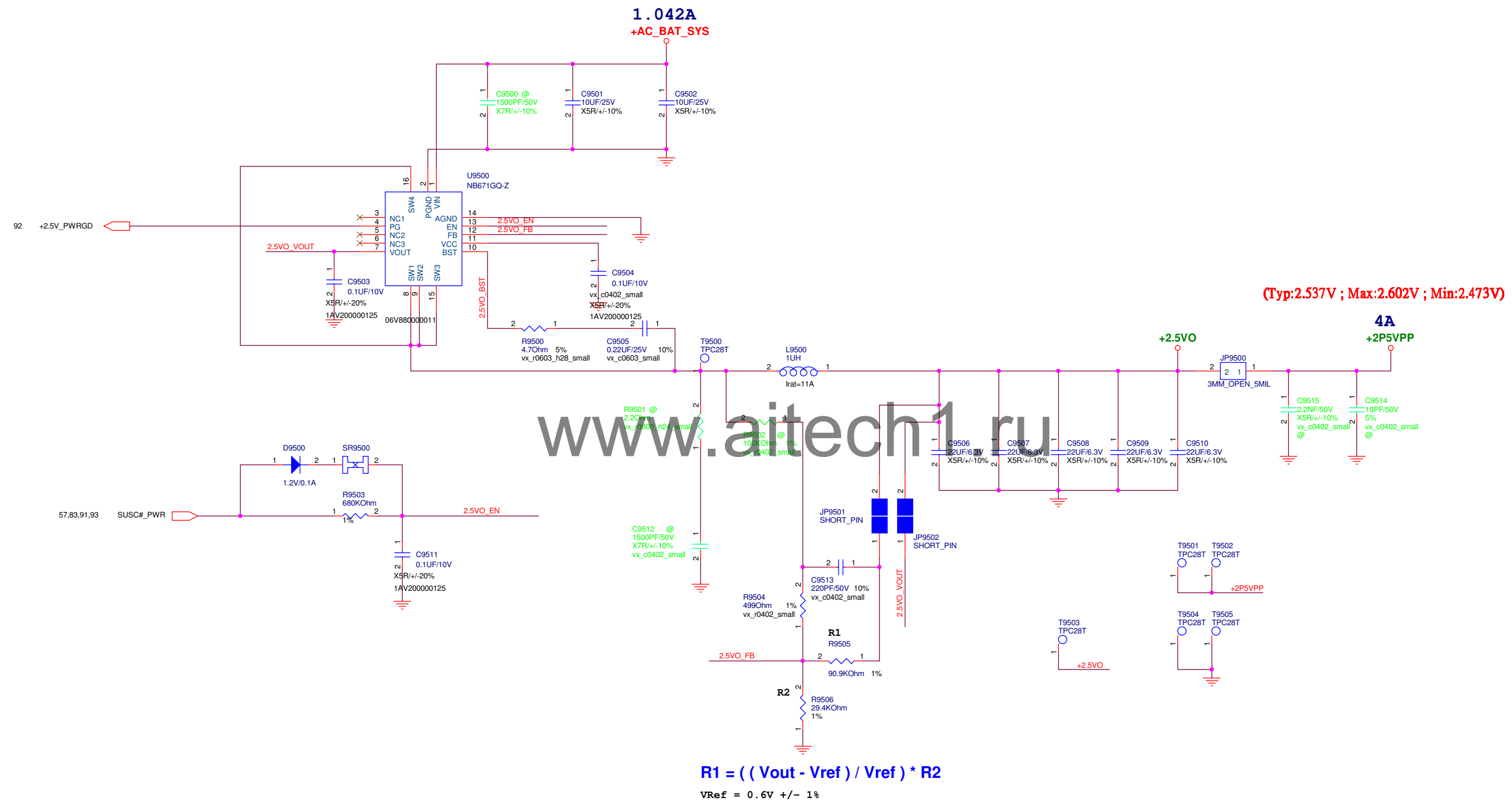
PEGATRON			Title : USB CHARGE IC		
Pegatron Corp.			Engineer: Shrek_Tseng		
Size Custom	Project Name IPPSL-CD				Rev A00
Date: Monday, October 17, 2016			Sheet 92 of 108		



FOR POWER TEST



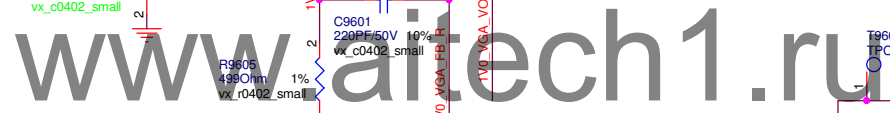
+2.5V POWER SUPPLY



$$R1 = ((V_{out} - V_{ref}) / V_{ref}) * R2$$

$$V_{Ref} = 0.6V \pm 1\%$$

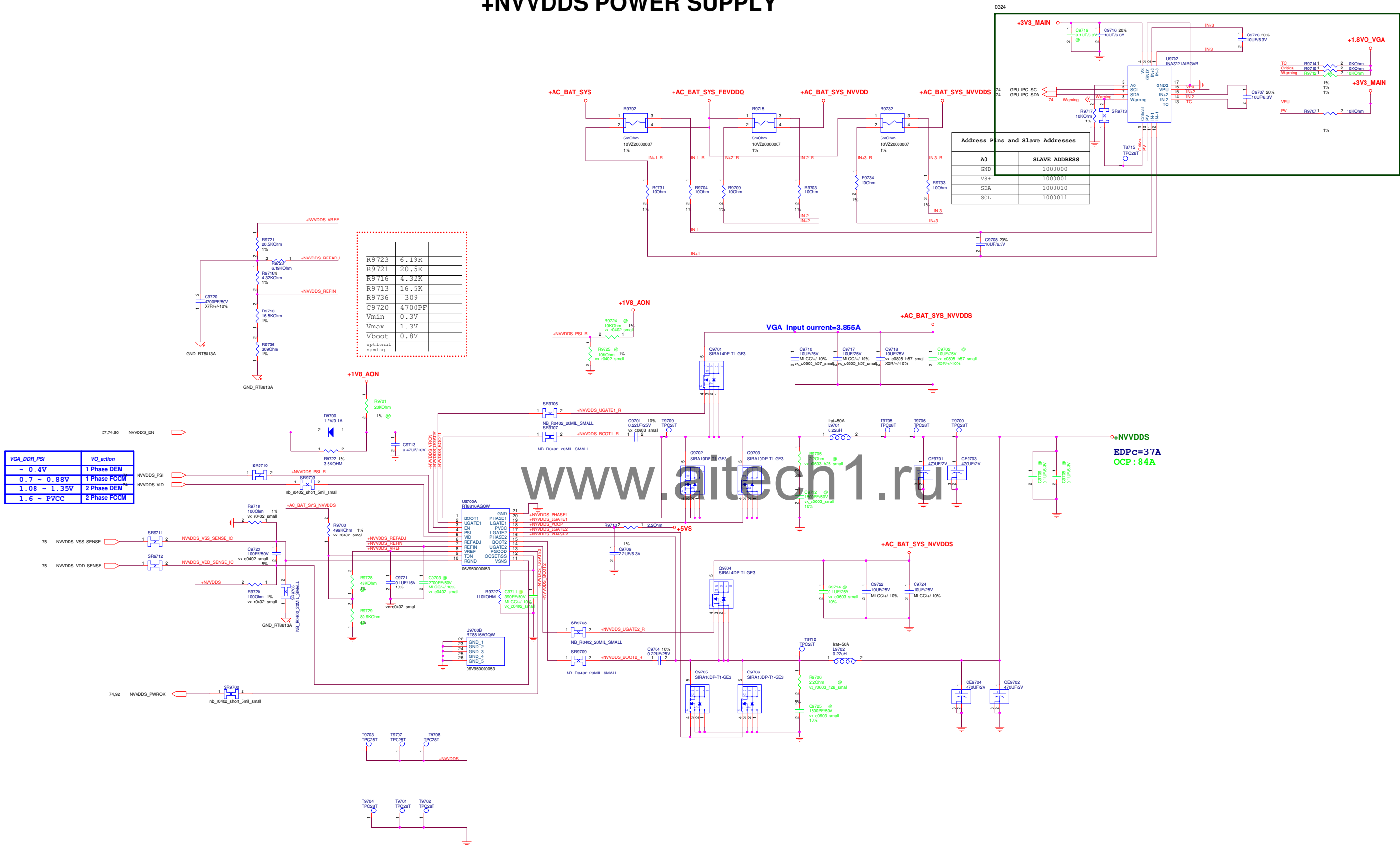
0.313A
+AC_BAT_SYS



$$R1 = ((V_{out} - V_{ref}) / V_{ref}) * R2$$

$$V_{Ref} = 0.6V \pm 1\%$$

+NVVDDS POWER SUPPLY



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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 98 of 101	

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016		Sheet 99 of 101	

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PEGATRON		Title : DDR3 TERMINATION A&B	
Pegatron Corp.		Engineer: Kai_Shen	
Size A	Project Name P7RCR		Rev R1.0
Date: Monday, October 17, 2016	Sheet 100 of 101		

